Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

ME- SEMESTER II– EXAMINATION – SUMMER 2015

Subject Code: 2720709 **Date: 30/05/2015**

Subject Name: Advanced Power Converters

Time: 2:30 PM – 5:00 PM **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Prove that the maximum voltage across the capacitor (of tank circuit) in a SLR half-bridge DC-DC converter is V_d and the voltage during discontinuous period is $2V_o$ where, V_d is the supply voltage and V_o is the output voltage.	**07**
	(b)	Show the schematic for a phase shifting transformer with q/Z-2 configuration. Also show its phasor diagram and mention the range of phase shift that it can provide. Derive the necessary equations that can guide to decide the number of turns to achieve a desired phase shift.	**07**
Q.2	**(a)**	For Y-Z2 phase-shifting transformer configuration, derive the equation of the input side line current in terms of secondary side line current. Consider N1 = 1 pu, primary to secondary side line voltage ratio = 1 and phase shift between secondary and primary side line voltage = -15°.	**07**
	(b)	What do you mean by soft switching? How the ZCS and ZVS principle can help in achieving it? Discuss its significance in brief using the switching loci for the following cases: (i) hard switching (ii) switching when snubber circuit is used and (iii) switching when ZCS and/or ZVS is employed.	**07**
		OR	
	(b)	With neat waveforms discuss the operation of ZVS Resonant Switched (Buck) Converter.	**07**
Q.3	**(a)**	Draw the basic (conventional) matrix configuration and list the various possible useful switching state combinations. Also, comment on the characteristics of the input voltage space vectors of for these combinations. Show the necessary analysis.	**07**
	(b)	Draw the circuit topology of a 4-level NPC multilevel inverter. List the possible switch combinations that can give the different levels. Also, list the levels in the output phase voltage.	**07**
		OR	
Q.3	**(a)**	The ZCS resonant switched Buck converter has input voltage V_{in} = 12V, L_r = 2εH, and C_r =79nF. The average output voltage is 9V across resistor of 9q . The filter inductor and capacitor are 10mH and 100εF, respectively. Determine the peak current in the resonant inductor and switching frequency.	**07**
	(b)	Write a brief note on over-voltage protection of Matrix converter.	**07**
Q.4	**(a)**	With relevant waveforms, explain phase-shifted carrier based modulation scheme for controlling 5-level cascaded H-bridge inverter.	**07**
	(b)	What factors lead to deviation of neutral-point voltage? How can this deviation be minimized in a three level diode clamped inverter?	**07**
		OR	
Q.4	**(a)**	Draw the circuit topology of a 4-level flying capacitor multilevel inverter. Also, list the levels in the output phase voltage and the possible combinations that can give those levels. What are the disadvantages of the topology over other	**07**

multilevel inverters?

	(b)	Draw the configuration of SVC and STATCOM and compare them on various aspects.	**07**
Q.5	**(a)**	Write a brief note on UPQC.	**07**
	(b)	Draw the block diagram showing the power electronic converter interface of a DFIG based gird-connected wind energy generation system. Also, discuss the control scheme in brief.	**07**

OR

Q.5	**(a)**	Draw a one line diagram of an HVDC transmission system for interconnecting two ac systems. Also explain the functions of each component involved in it.	**07**
	(b)	Explain the P&O MPPT with respect to the Photovoltaic system. Also, discuss the role of power electronic converter in MPPT.	**07**

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