Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

SEMESTER–EXAMINATION –

Subject code: 2722602 **Date:**

Subject Name: CMOS Circuit Design - II

Time: **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	In SC non-inverting amplifier (see Fig. 1, Q:1 (a)), S_1 turns off ϕt seconds after S_2 turns off, and S_3 turns on ϕt seconds after S_1 turns off. Plot the output waveform taking into the charge injection and clock feedthrough of all switches. Assume all switches are implemented with NMOS. Provide supportive explanation for the plot drawn by you.	**07**
	(b)	Draw and explain operation of multiply-by-two SC circuit. What should be sequence of operation of switches and why? Also draw its equivalent circuits for sampling and amplification phases.	**07**
Q.2	**(a)**	Show that the output noise voltage is approximately same as input-referred noise voltage of op amp in the voltage reference generator circuit shown in Fig. 2, Q:2 (a). Neglect parasitic capacitance C_B shown in the figure.	**07**
	(b)	How does the op-amp input offset voltage affect the output voltage in temperature independent voltage reference circuit? What are the solutions to solve this problem? Draw the final circuit which has the less effect of op-amp input offset voltage and feasible for implementation in CMOS technology.	**07**
		OR	
	(b)	**1.** Suppose a type I (simple) PLL experiences a frequency step ϕx at t = 0. Calculate the change in phase error using Laplace transform. **2.** In type I PLL, an external voltage V_{ex} is added to the output of low-pass filter. (a) Determine the phase error and V_{LPF} if the loop is locked and $V_{ex} = V_1$. (b) Suppose V_{ex} steps from V_1 to V_2 at $t = t_1$. How the PLL will respond?	**07**
Q.3	**(a)**	What do you understand by jitter? Show that the basic charge pump PLL behaves as low-pass filter for the jitter appearing in input signal and it behaves as high-pass filter for the jitter appearing in VCO signal.	**07**
	(b)	Draw cross section of floating memory element and explain its operation from the point of view of reading, writing and erasing.	**07**
		OR	
Q.3	**(a)**	Explain with necessary diagrams and waveforms, the issue observed in basic charge pump PLL due to finite capacitance seen at the drains of current sources. Suggest possible solution to this problem.	**07**
	(b)	In sensing flash memory using DSM, how can we dump a constant charge independent of bit line voltage into bit line capacitor? Draw necessary circuit diagram and explain its operation.	**07**
Q.4	**(a)**	Sketch a circuit for sensing resistive memory using a concept of DSM	**07**

and derive expression of R_{mbit}.

(b) Draw and explain the block diagram of voltage comparator. Discuss the operation of positive feedback decision circuit with necessary equations in detail. **07**

OR

Q.4 **(a)** Illustrate operation of sense amplifier having rail-to-rail input range. Discuss performance of the same from the point of view of kick-back noise, clock feed-through, power dissipation, and memory. **07**

(b) Describe operation CMOS analog multiplier along with circuit diagram and mathematical analysis. **07**

Q.5 **(a)** Sketch general implementation of charge scaling DAC and explain its working with necessary mathematical analysis. **07**

(b) Briefly discuss following parameters which play a critical role in the overall performance and design of LNA. **07**

1. Noise Figure
2. Input Return Loss
3. Stability

OR

Q.5 **(a)** Draw block diagram of dual slope ADC and explain its operation with necessary mathematical analysis. **07**

(b) List out various LNA topologies. Explain quantitatively operation of common source stage with inductive load LNA along with diagram. **07**

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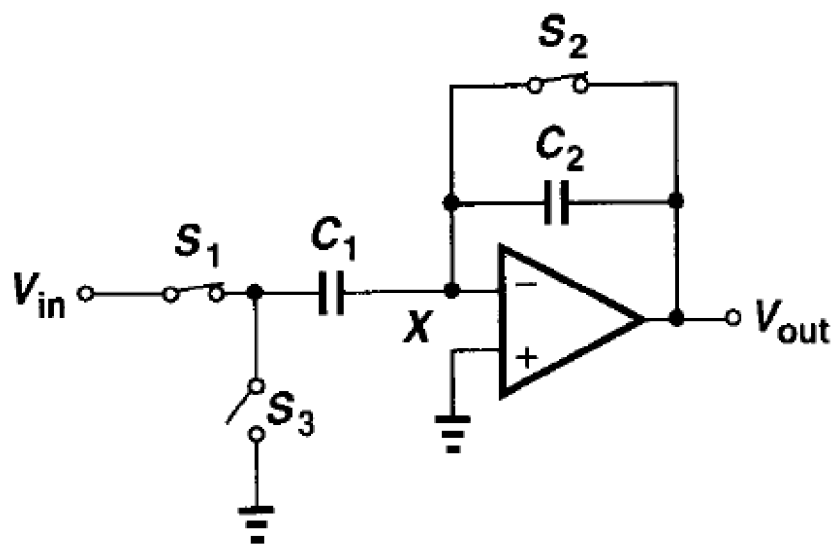

Fig. 1: Q:1 (a)

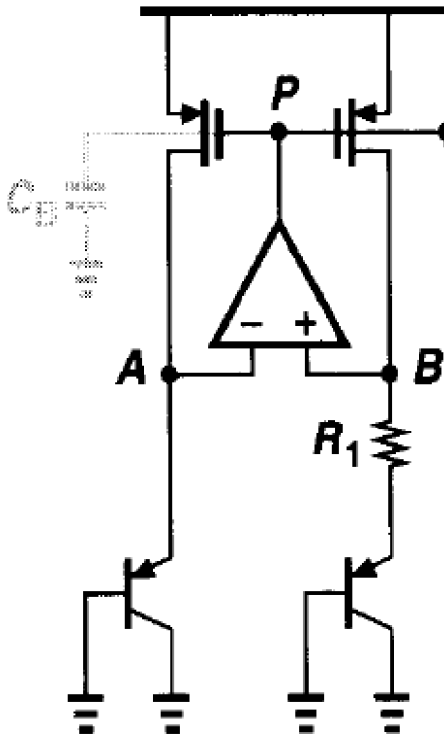

Fig. 2: Q:2 (a)