Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

ME- SEMESTER II– EXAMINATION – SUMMER 2015

Subject Code: 2722606 Date: 01/06/2015

Subject Name: Algorithms for VLSI Physical Design Automation

Time: 2:30 PM – 5:00 PM Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1 **(a)** Do as Directed: **07**

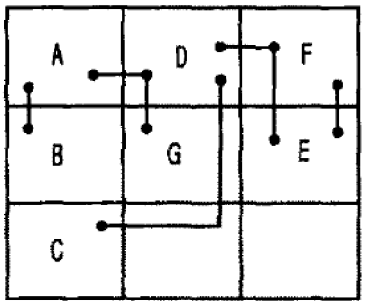
(i) Explain Sea of Gate **or** Channel less Gate array

(ii) How to process Unequal sized elements using Kernighan-Lin Algorithm?

(iii) Draw and explain Channel intersection graph.

(iv) Assuming that the capacity of each edge is 3 tracks, find D(P) the maximum ratio of nets assigned to each edge to the channel capacity, The signal nets for the circuit whose placement P is given in Figure below. Assume the weight of each net to be unity.

Comment on routability of P.



(v) Discuss limitations of Lee Algorithm for large circuits.

(vi) What do you mean by trunk and branch in channel routing?

(vii) Discuss sequential approach in Global routing.

(b) Consider the netlist given below: **07**

0 1 4 5 1 6 7 0 4 9 0 0

2 3 5 3 5 2 6 8 9 8 7 9

Using VCG, zone representation and HCG, minimize the longest path in the VCG by merging nodes of VCG. (i.e Apply Yoshimura Kuh algorithm on it.)

Q.2 **(a)** Discuss Cluster growth algorithm for Floorplanning in brief. **07**

(b) What are differences and similarities between Kernighan-Lin and Fiduccia-Mattheyses heuristics in reference to circuit partitioning problem? Discuss in brief. **07**

OR

(b) Discuss optimization of Standard- cell Layout. **07**

Q.3 **(a)** Enumerate various methods for Estimation of wirelength and describe any three in detail. **07**

(b) Discuss Hadlockôs algorithm. **07**

OR

Q.3	**(a)**	Draw and explain Micro- cell design style.	**07**
	(b)	Explain min-cut placement algorithm along with its limitations.	**07**
Q.4	**(a)**	Explain Genetic Algorithm in brief.	**07**
	(b)	Discuss Conversion algorithm for global routing.	**07**
		OR	
Q.4	**(a)**	Discuss constrained left-edge algorithm. What is its limitation?	**07**
	(b)	Discuss simulated annealing algorithm for circuit partitioning.	**07**
Q.5	**(a)**	Discuss Lee algorithm	**07**
	(b)	Explain in brief: 1. Adjacency Graph 2. PLA Folding	**07**
		OR	
Q.5	**(a)**	Draw levels of abstraction and corresponding design steps in VLSI design process. Also discuss difficulty associated with physical design.	**07**
	(b)	Discuss PLA personality and optimization for Layout.	**07**

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