Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

ME- SEMESTER II– EXAMINATION – SUMMER 2015

Subject Code : 2724202 **Date: 28/05/2015**

Subject Name: Testing& Verification of VLSI Design

Time: 2:30 PM – 5:00 PM **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Explain the following terms. I. Defect II. Error. III. Fault.	**07**
	(b)	Explain test economics.	**07**
Q.2	**(a)**	Explain the cost of bugs over a time.	**07**
	(b)	Justify the statement ñVerification is necessary evilò.	**07**
		OR	
	(b)	Discuss Functional Versus Structural Testing	**07**
Q.3	**(a)**	Explain the different verification styles in detail.	**07**
	(b)	Explain the following terms. I. Black Box verification. II. White Box verification. III. Gray Box verification.	**07**
		OR	
Q.3	**(a)**	List down different verification tool and explain any one in detail.	**07**
	(b)	What is the importance of function coverage in testing? Explain in detail.	**07**
Q.4	**(a)**	What do you mean by Design for Verification? Explain in detail.	**07**
	(b)	Explain the Role of testing for VLSI circuit.	**07**
		OR	
Q.4	**(a)**	What is Built in self test? Explain in detail.	**07**
	(b)	Discuss theory and Analysis of Linear Feed Back Shift Register.	**07**
Q.5	**(a)**	Explain the Tradeoff between Teacher and Student Risk with example.	**07**
	(b)	Explain the following terms. I. Testing. II. Verification.	**07**
		OR	
Q.5	**(a)**	Describe Complex D-Algorithm with Example.	**07**
	(b)	Describe Functional RAM Testing with March Tests.	07

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