Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

ME- SEMESTER II– EXAMINATION – SUMMER 2015

Subject Code: 2724204 **Date: 01/06/2015**

Subject Name: HDL Based Design with Programmable Logic

Time: 2:30 PM – 5:00 PM **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

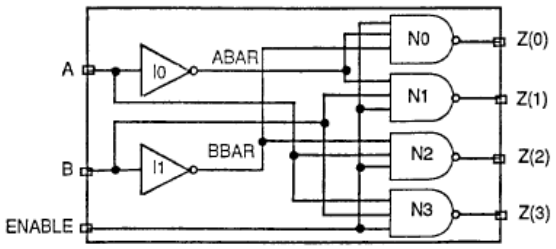
Q.1 **(a)** Do as directed. (1,2,3 each of 2 Marks, 4 of 1 Mark) **07**

1. Write a VHDL statement to declare a port with following attributes ï
   i. Port name: DATABUS
   ii. Width : 8bit (A_0, A_1 ,A_2, é , A_8)
2. Model a 3 i/p NAND gate with inertial delay of 5 ns? Draw the i/p ï o/p waveform.
3. How many logic levels are supported by STD_ULOGIC data type? Which of them are synthesizable?
4. Process statement can be used to describe sequential logic only. Justify whether the statement is True or False.

(b) Answer in short. (1,2,3 each of 2 marks, 4 of 1 mark) **07**

1. What are the four forms of explicit wait condition?
2. What are the advantages of HDL based digital design entry compared to conventional schematic based design entry?
3. Differentiate between *Transaction* and *Event* with suitable example in digital design using HDL.
4. Declare a memory data type of 8 registers with size of each register 32 bits.

Q.2 **(a)** Write the behavioral VHDL code to describe the given combinational circuit using PROCESS statement. **07**



(b) 1. List and discuss the level of abstractions at which the Digital circuit can be described. Comment on the accuracy vs. speed of simulation at each abstraction level. (4 Marks) **07**

2. Discuss different VLSI Design Styles in use for implementing digital logic on Integrated Circuits. (3 Marks)

OR

(b) What is the use of EDA tools? List the name of the companies in the business of developing EDA tools for VLSI. What is the role of following EDA tools in FPGA based logic design? **07**

a. Behavioral Synthesis
b. RTL Synthesis
c. Translate
d. Mapping
e. Place and Route (PAR)

Q.3 **(a)** Prepare the PLA programming table to realize following Boolean functions. Draw the structure of the programmed PLA to produce normal output. Calculate the total number of programmable links of the PLA. **07**

$$F_1 = \sum(3,4,6,7)$$
$$F_2 = \prod(0,1,3,5,7)$$
$$F_3' = \sum(5,7)$$

(b) Draw and explain the basic architecture of FPGA. What are the advance features available in current FPGA devices? **07**

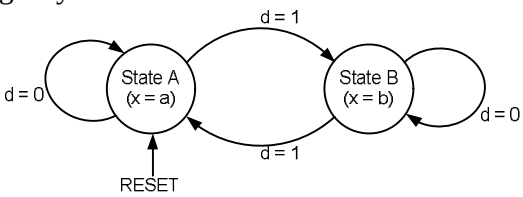
OR

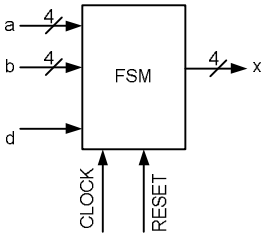
Q.3 **(a)** What is the basic building block of any CPLD? Draw and explain the construction of any standard CPLD device? **07**

(b) Optimize the Boolean function $F = A + B + ACD$ for minimum hardware and then implement F using 2x1 MUX as well as 2 i/p LUT. Write the behavioral VHDL code (architecture only) for implementing F . **07**

Q.4 **(a)** Define Event-Driven Simulator and Cycle-Based Simulators. Discuss the operation of event based simulator with suitable example. **07**

(b) Write a VHDL description for the state machine given below using FSM design style. **07**

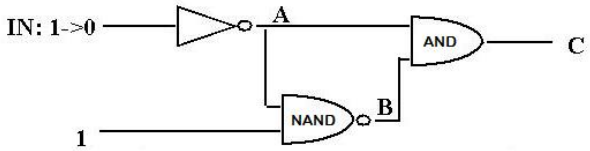




OR

Q.4 **(a)** **07**

1. What is synthesis? How behavioral synthesis is different from RTL synthesis? (3 Marks)
2. Explain the activity at node C in reference to delta-delay simulation in VHDL. How many deltas are needed to evaluate C? (4 Marks)



(b) Describe a decade counter in VHDL using FSM technique which will count up at every positive edge of the clock. If RESET is asserted, counter should start from zero. **07**

Q.5 **(a)** What is HDL? Discuss the relative differences between two widely used HDLs - VHDL and Verilog. **07**

(b) Write VHDL description for negative edge triggered 4-bit shift register with active low asynchronous *LOAD* input, which should load the register with binary pattern ñ1110ò. If *DIR* i/p is ó1ô then perform shift left else shift right operation. *DIR* is synchronous i/p. **07**

OR

Q.5	**(a)**	Explain following VHDL constructs ï a. GUARDED BLOCK Statement b. GENERATE Statement	**07**
	(b)	Discuss the issues to be taken care while modeling the simulation in VHDL.	**07**

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