Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

ME - SEMESTER–II EXAMINATION – SUMMER 2015

Subject Code: 2724209 **Date: 30/05/2015**

Subject Name: VLSI Signal Processing

Time: 02:30 PM to 05:00 PM **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Define Following. 1. Iteration 2. Iteration Period 3. Loop Bound 4. Critical Loop 5. Acyclic Precedence Graph 6. Cutset 7. Feed Forward Cutset	**07**
	(b)	Which are the DSP Algorithms used for implementation of DSP Systems? Discuss its applications.	**07**
Q.2	**(a)**	What is Fine-Grain Pipelining? How it is used in FIR Filters?	**07**
	(b)	Discuss the Properties of Retiming.	**07**
		OR	
	(b)	Explain Bit Level Parallel Processing in brief.	**07**
Q.3	**(a)**	Briefly explain the algorithm of unfolding.	**07**
	(b)	Compare Pipelining & Parallel Processing for VSP.	**07**
		OR	
Q.3	**(a)**	Which are the Power Reduction Techniques? Discuss its role in DSP Systems.	**07**
	(b)	What is the role of scaling in VLSI Signal Processing? Briefly explain it.	**07**
Q.4	**(a)**	Explain Fast convolution.	**07**
	(b)	Explain Multirate Systems using example.	**07**
		OR	
Q.4	**(a)**	Discuss Systolic Design Methodology. Compare it with other Methodology.	**07**
	(b)	Draw Transposed SFG & Data Broadcast Structure of 3 Tap FIR Filter.	**07**
Q.5	**(a)**	Write a note on Wave Pipelining.	**07**
	(b)	Discuss Redundant Number Representation.	**07**
		OR	
Q.5	**(a)**	Write a note on DSP Processors.	**07**
	(b)	Briefly explain how Distributed Arithmetic Architectures can be used in VLSI Signal Processing?	**07**

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