Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

ME - SEMESTER– II • EXAMINATION – SUMMER 2015

Subject Code: 2725204 **Date: 29/05/2015**

Subject Name: Designing with Modeling & FPGA's

Time:02:30 PM To 05:00 PM **Total Marks: 70**

Instructions:

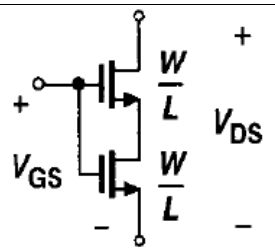
1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1 **(a)** Write short notes on two of the following: **07**

i. Channel Length Modulation

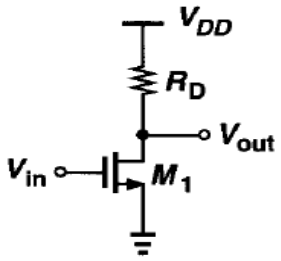
ii. Sub Threshold Conduction

(b) **07**

	Consider the structure shown in Figure. Determine I_D as a function of Vgs and Vds and Prove that the structure can be viewed as a single transistor having as aspect ratio W/(2L).Assume $\lambda=\Upsilon=0$.

Q.2 **(a)** In CS stage with source Degeneration configuration, explain how we obtain voltage gain? And derive same (voltage gain) with equivalent circuit? **07**

(b) In the circuit of common-source stage, assume $(W/L)_1=50/0.5, R_D=2k\Omega$ and $\lambda=0$. **07**

	(i)What is the small-signal gain if M_1 is in saturation and I_D=1mA? (ii)What input voltage place M_1 at the edge of the triode region? What is the small-signal gain under this condition?

OR

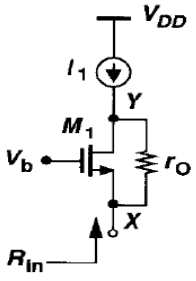
(b) In case differential pair, drive the expression for small- signal voltage gain? Plot the input-output characteristic of a differential pair as device width and the tail current vary and discussed. **07**

Q.3 **(a)** How we can resolve the issue of inaccuracy in cascade current mirror due body effect? **07**

(b) What are types of feedback topologies? Briefly explain with diagram. **07**

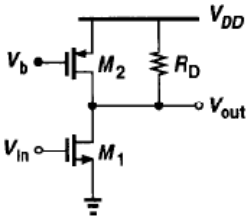
OR

Q.3 **(a)**



Calculate the input resistance of the circuit using Miller's theorem. **07**

(b) **07**



Calculate the input-referred 1/f and thermal noise voltage of the circuit depicted in figure assuming M1 and M2 are in saturation.

Q.4 **(a)** What are advantages of two stages Op-amp over one stage op-amp? Discuss gain boosting circuit working? **07**

(b) CMFB using triode devices suffers with limited output voltage swings, how can this issue resolved? **07**

OR

Q.4 **(a)** What is drawback of telescopic cascades, that make is the difficult the input output shorting. Draw circuit diagram of folded cascade op-amp with cascade PMOS loads and discuss advantages over folded cascade op amp topology. **07**

(b) Discuss the operation of MOSFETS as switches (switched-capacitor)? **07**

Q.5 **(a)** What is difference between Negative-TC voltage and Positive-TC voltage? Draw circuit for bandgap reference and discuss its operation. Discuss its compatibility with CMOS Technology. **07**

(b) Explain Switched-capacitor Integrator? **07**

OR

Q.5 **(a)** What is PLL? Discuss its block diagram, working, operation principle. What are applications of PLL? **07**

(b) Write short note on any two (i)Binary weighted Resister(ii)R-2R Ladder(iii)Multiplier DAC&(iv) Non-Multiplier DAC **07**

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