

GUJARAT TECHNOLOGICAL UNIVERSITY**ME - SEMESTER– I (New course)• REMEDIAL EXAMINATION – SUMMER 2015****Subject Code: 3715204****Date:16/05/2015****Subject Name: Digital VLSI Design & Verification-I****Time: 10:30 am to 1:00 pm****Total Marks: 70****Instructions:**

1. Attempt all questions.
2. Make suitable assumptions wherever necessary.
3. Figures to the right indicate full marks.

- Q.1** (a) What is FSM? Design FSM to detect the sequence 1011. **07**
 (b) Explain function and task in Verilog with example? **07**

- Q.2** (a) Design JK flip flop to D flip flop conversion? **07**
 (b) What is test bench? Explain with example? **07**

OR

- (b) Design full adder using 4 to 1 multiplexer and write the Verilog code for full adder. **07**

- Q.3** (a) What is metastability? When/why it will occur? Explain the different ways to avoid? **07**
 (b) Explain different design abstraction levels with one example? **07**

OR

- Q.3** (a) What is FIFO? Explain with diagram. **07**
 (b) Explain ASIC design flow? **07**

- Q.4** (a) What is delta simulation time in VHDL? Explain with example? **07**
 (b) Write short note on soft cores, Firm cores and hard cores. **07**

OR

- Q.4** (a) What is CLB in FPGA? Explain with block diagram. **07**
 (b) Write short note on **07**
 I. Nonrecurring engineering cost and recurring cost.
 II. Yield and technology scaling.

- Q.5** (a) What is verification? Explain the difference between direct testing and constrained random verification. **07**
 (b) Explain the maximum clock frequency of a digital circuit by taking one suitable example. **07**

OR

- Q.5** (a) Write a note on clock gating. **07**
 (b) Explain the noise margin with diagram. **07**
