Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

ME - SEMESTER– I (OLD course)• EXAMINATION – SUMMER 2015

Subject Code: 710305 **Date:15/05/2015**

Subject Name: PROGRAMMABLE LOGIC CONTROLLER

Time: 10:30 am to 1:00 pm **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Draw the block diagram of PLC and explain each block in brief.	**07**
	(b)	Explain the purpose of electrical isolation at input and output modules of PLC and explain input module layout with diagram.	**07**
Q.2	**(a)**	Draw a schematic of PLC memory organization. Determine memory size needed for a programmable controller system with 300 input points and 200 output points (assume 30 % spare memory capacity).	**07**
	(b)	Explain Delay ON Timer in PLC with suitable examples and timing diagrams.	**07**
		OR	
	(b)	Explain Delay OFF Timer instruction in PLC with suitable example.	**07**
Q.3	**(a)**	Brief about classification of PLC based on I/O count and housing. State the advantages and disadvantages of PLC system.	**07**
	(b)	Explain SKIP and MCR (Master Control Relay) in PLC in detail.	**07**
		OR	
Q.3	**(a)**	Brief about sourcing and sinking in context of PLC system.	**07**
	(b)	Discuss the Shift Registers Function in PLC and brief about possible applications.	**07**
Q.4	**(a)**	The Pressure transmitter, which transmits 4 to 20 mA current, is connected with analog input module of PLC through 20 AWG wire (Resistance 10 Ý/1000). The distance between the PT and PLC is 3000'. Calculate the total loop resistance and voltage drop in wire when input transmitter send maximize current to PLC. Also show the wiring diagram for the above system.	**07**
	(b)	A railway station has 3 platforms A, B and C. A train is coming into the station. It has to be given entry to platform A if A is empty. If both A and B are occupied then it has to be given entry to platform C. If all the platforms are full then the train has to wait. Show truth table and design the necessary logic diagram.	**07**
		OR	
Q.4	**(a)**	Design a ladder diagram that will control a stepper motor so that it moves 10 steps forward, wait for 20 seconds, and then cause the motor to move 10 steps in reverse direction.	**07**
	(b)	Design a simple timing circuit that can be used to generate an alternating signal to produce flashing alarm light connected to output at bit location O:002/005.	**07**
Q.5	**(a)**	Brief about sequencer functions of PLC. Explain cascading sequencer with an example.	**07**
	(b)	Explain PLC jump instruction in detail.	**07**
		OR	
Q.5	**(a)**	Brief about any two special function modules of PLC.	**07**
	(b)	Brief about PLC comparison functions.	**07**