Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

ME - SEMESTER– I (OLD course)• EXAMINATION – SUMMER 2015

Subject Code: 710403 **Date:13/05/2015**

Subject Name: ASIC Design

Time: 10:30 am to 1:00 pm Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1		Do as directed. (Two marks each)	**14**
	1	Explain the importance of Regularity for chip design.	
	2	Discuss physical data type with examples as used in VHDL.	
	3	What is the difference between STD_LOGIC and STD_ULOGIC?	
	4	Explain variable in VHDL.	
	5	State importance of configuration.	
	6	Explain positional association and named association in the port map clause.	
	7	Write entity declaration for 1x4 de-multiplexer.	
Q.2	**(a)**	Draw state diagram and write VHDL code for ñ10ò sequence detector using both moore and mealy FSM.	**07**
	(b)	With flow diagram explain ASIC design methodology.	**07**
		OR	
	(b)	Give comparison between CPLD and FPGA with diagram.	**07**
Q.3	**(a)**	Write down the VHDL code for 4x1 multiplexer using when else construct. Using same draw diagram and write VHDL code to implement 16x1 multiplexer using structural modeling.	**07**
	(b)	Write VHDL code for an 8-bit Switch tail counter. It is an 8-bit shift register, where the bit 0 is inverted and fed to the D input of the bit 7. When initialized with 00000000, the sequence is 10000000, 11000000, 11100000é 00000011, 00000001.	**07**
		OR	
Q.3	**(a)**	Write VHDL code for 2x4 decoder using process. Using 2x4 decoder draw and write VHDL code to implement 3x8 decoder using structural modeling.	**07**
	(b)	Write VHDL code for 4 bit shift right register using generate statement.	**07**
Q.4	**(a)**	Draw programmable logic array (PLA) and explain implementation of 1 bit full adder using same.	**07**
	(b)	Explain test bench with appropriate example.	**07**
		OR	
Q.4	**(a)**	Realize the following functions using PAL. F1= Ém (3,4,5,6,7,10,13,15) F2= Ém (2,4,6,8,10,14,15) F3= Ém (5,7,13,15)	**07**
	(b)	Discuss fuse, antifuse and SRAM programming methods of FPGA.	**07**
Q.5	**(a)**	Write short note on Various Loops in VHDL	**07**
	(b)	Write a short note on package and library.	**07**
		OR	
Q.5	**(a)**	Discuss following with appropriate examples. (i) Wait statements (ii) Exit statement (iii) Next statement	**06**
	(b)	Explain inertial delay and transport delay with appropriate example.	**04**
	(c)	Discuss the predefined operators in VHDL	**04**

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