

Seat No.: \_\_\_\_\_

Enrolment No. \_\_\_\_\_

## GUJARAT TECHNOLOGICAL UNIVERSITY

ME - SEMESTER- I (OLD course) • EXAMINATION – SUMMER 2015

Subject Code: 710412

Date: 16/05/2015

Subject Name: Digital VLSI Design

Time: 10:30 am to 1:00 pm

Total Marks: 70

Instructions:

1. Attempt all questions.
2. Make suitable assumptions wherever necessary.
3. Figures to the right indicate full marks.

- Q.1 (a) Explain CMOS n-Well fabrication process with necessary diagram. 07  
(b) Discuss the each three domain of Y-chart in detail. 07
- Q.2 (a) Derive the MOSFET drain current equation while MOSFET is operating in linear region. Draw the current-voltage characteristics of the MOSFET and explain in detail. 07  
(b) Explain two types of scaling with its advantages and disadvantages. 07
- OR
- (b) Calculate the threshold voltage  $V_{TO}$  at  $V_{SB} = 0$ , for a polysilicon gate n-channel MOS transistor, with the following parameters: substrate doping density  $N_A = 10^{16} \text{ cm}^{-3}$ , polysilicon gate doping density  $N_D = 2 \times 10^{20} \text{ cm}^{-3}$ , gate oxide thickness  $t_{ox} = 500 \text{ \AA}$ , and oxide-interface fixed charge density  $N_{ox} = 4 \times 10^{10} \text{ cm}^{-2}$ . Assume  $n_i = 1.45 \times 10^{10} \text{ cm}^{-3}$ ,  $\phi_{F(\text{gate})} = 0.55 \text{ V}$ ,  $\epsilon_{ox} = 3.97\epsilon_0$ ,  $\epsilon_{si} = 11.7\epsilon_0$ ,  $\epsilon_0 = 8.85 \times 10^{-14} \text{ F/cm}$ . 07
- Q.3 (a) Derive expressions for  $V_{IH}$  and  $V_{IL}$  for CMOS Inverter. 07  
(b) Write Short note on CMOS Transmission gate. 07
- OR
- Q.3 (a) Derive expressions for  $V_{IH}$  and  $V_{IL}$  for depletion-type nMOS Inverter. 07  
(b) Write a detail note on Oxide related MOSFET Capacitances. 07
- Q.4 (a) Write short note on Complementary Pass Transistor Logic (CPL). 07  
(b) What is clock skew problem for NP-Domino CMOS Logic circuits? Explain True Single Phase Clock (TSPC) Dynamic CMOS Logic circuits. 07
- OR
- Q.4 (a) Explain interconnect parasitics estimation with proper diagram. 07  
(b) Explain three stage CMOS ring Oscillator in detail. 07
- Q.5 (a) Explain the charge sharing problem in DOMINO CMOS logic. How it can be overcome, suggest simple solution. 07  
(b) Explain Voltage Bootstrapping with necessary diagram. 07
- OR
- Q.5 (a) Explain with circuit two input CMOS NOR and NAND gate. Also derive threshold voltage for both. 07  
(b) With diagram explain 1-bit full adder using transmission gates. 07