Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

ME - SEMESTER– III • EXAMINATION – SUMMER 2015

Subject Code: 730303 **Date:02/05/2015**

Subject Name: VLSI Design

Time: 2:30 pm to 5:00 pm **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Explain the typical design flow of Verilog HDL.	**07**
	(b)	Write a program to implement full adder using two half adders.	**07**
Q.2	**(a)**	Explain features of Spartan3e FPGA family in brief.	**07**
	(b)	Explain the use of casex, casez in verilog with example.	**07**
		OR	
	(b)	Write a Verilog code for 4-bit comparator.	**07**
Q.3	**(a)**	Design and write Verilog HDL code for Negative Edge Triggered D flip-flop.	**07**
	(b)	Write Verilog code for 1x8 demultiplexer.	**07**
		OR	
Q.3	**(a)**	Write a verilog code for 3-to-8 decoder with enable input.	**07**
	(b)	Write a program to implement 4-bit ripple carry counter.	**07**
Q.4	**(a)**	What is race condition in verilog? How it can be eliminated?	**07**
	(b)	List out the different types of operator and explain any three in details with example.	**07**
		OR	
Q.4	**(a)**	Write a verilog program for 8x1 Multiplexer using case statement.	**07**
	(b)	Consider Mealy Finite State Machine (FSM), with one input X and one output Z. The FSM asserts its output Z when it recognize the "111" input bit sequence. Implement the state diagram for above and write verilog code for it.	**07**
Q.5	**(a)**	With the help of T-flip flop design a modulo 8 counter. Show all design steps. Write verilog program of the same using structural model style. Also write verilog program of all components and draw the necessary diagram.	**14**
		OR	
Q.5	**(a)**	Explain methodology of digital design along with neat sketch.	**03**
	(b)	Explain port connection rules in terms of module.	**04**
	(c)	Compare between 1.FPGA & CPLD 2. PLA & PLD	**07**

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