Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

ME - SEMESTER– IV • EXAMINATION – SUMMER 2015

Subject Code: 740301 **Date: 01/05/2015**

Subject Name: Advanced VLSI Design

Time: 2:30 pm to 5:00 pm **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1 Implement the function $Z = X^3 + Y^3$ in verilog considering maximum time delay in the critical path of one 8 bit x 8 bit multiplier delay only. Assume Z, X, and Y of 8-bit. Write verilog code and draw implementation diagram of the same. What is the throughput and latency of your design? **14**

Q.2 (a) Write verilog code and draw implementation diagram to implement the boolean function Z= (X1+X2+X3+X4) X5 considering timing as the optimization criteria. Justify your design. What are the throughput, latency and timing of your design? How? **07**

(b) What is the advantage and limitation of using dual edge triggered flip-flops? Write verilog code of dual edge triggered T flip-flop having asynchronous reset. **07**

OR

(b) Draw the interface between burstable memory and a PCI bus, and explain First-In-First-Out (FIFO) structure using handshaking signals. **07**

Q.3 (a) Draw RTL implementations for the given verilog codes and justify your implementations. **06**

(i)
```
always @(posedge clk) begin
        L <= a1 & a2;
        out <= L | a3;
  end
```

(ii)
```
always @(posedge clk) begin
        L = a1 & a2;
        out = L | a3;
  end
```

(b) Draw timing diagram that shows all signals observed in simulation window while checking functionality of implementation of x^5 using pipelined architecture. Write Verilog code of the same. State throughput, latency and timing of this design. **08**

OR

Q.3 **(a)** Draw RTL implementations for the given verilog codes and justify your implementations. **06**

(i)
```
always @(posedge clk) begin
        out = L | a3;
        L = a1 & a2;
end
```

(ii)
```
reg y;
assign out = y;
    always @(clk)
        y = out ^ clk;
    end
```

(b) Draw timing diagram that shows all signals observed in simulation window while checking functionality of implementation of x^5 using iterative architecture. Write Verilog code of the same. State throughput, latency and timing of this design. **08**

Q.4 **(a)** Implement the Boolean function Y= [{x1 (x3' + x2)}+ x5'] x4 using minimum area as an optimization criteria. Consider that synchronous set and reset D-flipflops are available as the FDS element in the device. Write verilog code and implementation diagram of the same. What are the throughput, latency and timing of your design? How? **07**

(b) Draw RTL implementation for the given verilog code and justify your implementation. **07**

```
always @ (posedge clk) begin
        if(ctrl1) y<= ip1;
        if(ctrl2) y<= ip2;
end
```

OR

Q.4 **(a)** What is the disadvantage of resource sharing? Draw RTL implementation for the given code with and without resource sharing option. **07**

```
assign Y = (sel = = 0) ? i1+i2 : (sel = = 1) ? i1+i3 : i2+i3;
```

(b) What is the cause of static hazard on an asynchronous reset? With the help of necessary waveforms explain static-1 hazard condition while generating active low reset signal given by reset <= x1x2 + x2'x3. Give your suggestion to improve the design to prevent this hazard. **07**

Q.5 **(a)** With the help of verilog code and implementation diagram explain simple FSM and safe mode operated FSM. **07**

(b) What do you mean by static timing analysis? Explain positive slack and negative slack with the help of waveforms. **07**

OR

Q.5 **(a)** With the help of figures explain different methods to optimize floor planning. **07**

(b) Why fully asynchronous reset is not preferred? Write verilog code for the asynchronous reset and justify your answer with the help of waveforms. **07**

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