Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

ME - SEMESTER–IV • EXAMINATION – SUMMER 2015

Subject Code: 742601 Date: 01/05/2015

Subject Name: VLSI Test Principles and Architectures

Time: 2:30 pm to 5:00 pm Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	What do you understand by stuck-at-faults? Draw half-adder circuit and discuss all possible stuck-at-faults for this circuit as well as find a set of optimum test vectors to detect these stuck-at-faults.	**07**
	(b)	Discuss all possible transistor faults in two-input CMOS NAND gate and the method of testing each of them.	**07**
Q.2	**(a)**	Draw Muxed-D scan cell and explain full-scan design approach (architecture) using this scan cell. Take suitable circuit at block diagram level to describe various test operations.	**07**
	(b)	List out general scan design rules (part of checking and violation step) and explain any three of them in detail with suitable schematics.	**07**
		OR	
	(b)	What are the different steps involved in scan synthesis? Explain various decisions taken and modifications made to the circuit in scan configuration step.	**07**
Q.3	**(a)**	What is the meaning of event driven simulation? Explain zero-event driven simulation with the help of example. Draw necessary flow chart for the same.	**07**
	(b)	Discuss the term fault simulation. Explain parallel-fault simulation approach.	**07**
		OR	
Q.3	**(a)**	Explain the term hazard. Describe the approach to detect static hazard.	**07**
	(b)	What are the merits of deductive fault simulation? Discuss this approach in detail taking suitable example circuit.	**07**
Q.4	**(a)**	How does PODEM algorithm different from the D algorithm? Explain PODEM algorithm.	**07**
	(b)	Describe mixed-mode and hybrid BIST approaches to enhance fault coverage.	**07**
		OR	
Q.4	**(a)**	Discuss ATPG from the point of view of path-delay faults.	**07**
	(b)	Explain serial signature analysis output response compaction technique.	**07**
Q.5	**(a)**	List out various BIST design rules. Explain any four of them with necessary diagrams.	**07**
	(b)	Explain the term soft error and discuss how error-resilient scan approach addresses soft error issue.	**07**

OR

Q.5	**(a)**	Describe genetic algorithm based ATPG.	**07**
	(b)	Which scan design approach facilitates to test delay fault? Discuss its working in detail with suitable diagram. What are its disadvantages?	**07**

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