Seat No.: _____ Enrolment No._____

# GUJARAT TECHNOLOGICAL UNIVERSITY

**M.E –II$^{st}$ SEMESTER–EXAMINATION – JULY- 2012**

**Subject code: 1710412** **Date: 12/07/2012**

**Subject Name: Digital VLSI Design**

**Time: 10:30 am – 13:00 pm** **Total Marks: 70**

## Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

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|---|---|---|---|
| **Q.1** | | Answer the following questions (Two marks each) | **14** |
| | **(a)** | Draw 2x1 MUX using transmission gate. | |
| | **(b)** | Define work function for electron. | |
| | **(c)** | Explain crosstalk. | |
| | **(d)** | State importance of Euler path. | |
| | **(e)** | Let resistance and capacitance of transistor are R and C respectively. If width of transistor increase by factor k identify new value of resistance and capacitance in terms of R and C. | |
| | **(f)** | What do you mean by feature size and design rules? | |
| | **(g)** | Compare size, power dissipation and speed of SRAM and DRAM cell. | |
| **Q.2** | **(a)** | Draw and explain voltage transfer characteristic of CMOS inverter and discuss noise immunity and noise margin. | **07** |
| | **(b)** | Discuss device isolation technique which is used during fabrication. | **07** |
| | | **OR** | |
| | **(b)** | Explain types of photoresists and their usage in lithography process with appropriate diagram. | **07** |
| **Q.3** | **(a)** | What do you mean by MOSFET Scaling? Explain Constant-field Scaling and Constant-voltage Scaling in detail. | **07** |
| | **(b)** | Derive the equation for threshold voltage for a poly-silicon gate n-channel MOS transistor. | **07** |
| | | **OR** | |
| **Q.3** | **(a)** | Derive the equation of Drain current $I_D$ for an n-channel MOSFET operating in a linear region. | **07** |
| | **(b)** | Sketch 2 input NAND gate with transistor widths chosen to achieve effective rise and fall resistance equal to a unit inverter. Compute the rising and falling propagation delays in terms of R and C of the NAND gate driving h identical NAND gates using the Elmore delay model. If C = 2fF/µm and R = 2.5KΩ · µm in a 180nm process, what is the delay of fanout-of-4 NAND gate? | **07** |
| **Q.4** | **(a)** | Sketch transistor level schematic for a single stage CMOS logic gate for Boolean expression shown below and draw RC delay model. $Y = \overline{(A + B)\,C}$ | **07** |
| | **(b)** | Consider 5mm long, 0.32µm wide metal2 wire in 180nm process. The sheet resistance is 0.05Ω/□ and the capacitance is 0.2fF/µm. Estimate resistance and capacitance of the wire and construct a 3-segment π-model for the wire. A 4x unit-sized inverter drives a 2x inverter at the end of the 4mm wire. The gate capacitance is C = 5fF/µm and the effective resistance is R = 1.5KΩ · µm for nMOS transistors. Neglect diffusion capacitance. Estimate the propagation delay using Elmore delay model. | **07** |
| | | **OR** | |
| **Q.4** | **(a)** | For CMOS inverter, derive expression for propagation delay. | **07** |
| **Q.4** | **(b)** | Discuss basic principles of pass transistor circuits. | **07** |
| **Q.5** | **(a)** | Compare static and dynamic NAND gate with appropriate diagram. | **07** |
| | **(b)** | Draw the circuit diagram and stick diagram of 2-input CMOS NOR gate. | **07** |
| | | **OR** | |
| **Q.5** | **(a)** | Draw and explain CMOS SR latch circuit based on NOR2 gates. | **07** |
| | **(b)** | Compare and contrast static, dynamic and domino logic circuits. | **07** |

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