Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

M.E –IIst SEMESTER–EXAMINATION – JULY- 2012

Subject code: 1724201 **Date: 06/07/2012**

Subject Name: Power Efficient VLSI Design

Time: 10:30 am – 13:00 pm **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Compare SPICE simulation v/s Statistical based power estimation techniques.	**07**
	(b)	Discuss the significance of N-well process in low power design.	**07**
Q.2	**(a)**	The Chip Size of a CPU is 15mm x 25mm with clock frequency of 300MHz operating at 3.3V. The length of the clock routing is estimated to be twice the circumference of the chip. Assume that the clock signal is routed on a metal layer with width of 1.2 μm and the parasitic capacitance of the metal layer is 1fF/μm^2 . What is the power dissipation of the clock signal?	**07**
	(b)	Explain the significance of low power in VLSI design. Discuss the sources of power dissipation responsible for the failure.	**07**
		OR	
	(b)	Explain Twin Tub Process? Why high concentration of n-well is required?	**07**
Q.3	**(a)**	Explain use of proper isolation scheme to reduce parasitic in low power VLSI.	**07**
	(b)	Discuss Power and Performance Management.	**07**
		OR	
Q.3	**(a)**	Discuss different types of clock driving scheme with reference to their merits and demerits.	**07**
	(b)	Discuss Transition Density Signal Model.	**07**
Q.4	**(a)**	Discuss the significance of Power Delay Product.	**07**
	(b)	What is glitch? Explain various methods for glitch reduction in brief.	**07**
		OR	
Q.4	**(a)**	What is the significance of parallel and pipelining Architectures for low power design?	**07**
	(b)	Discuss the effect of process variation in the performance of clock distribution network.	**07**
Q.5	**(a)**	Compare Single Driver v/s Distributed Buffer scheme.	**07**
	(b)	Explain in detail different clock distribution network.	**07**
		OR	
Q.5	**(a)**	Discuss SRB Techniques for static power reduction.	**07**
	(b)	Discuss Multi –V_T Technique.	**07**

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