Seat N	lo.: _	Enrolment No.	Enrolment No	
GUJARAT TEC		GUJARAT TECHNOLOGICAL UNIVERSITY		
		M.E –I st SEMESTER–EXAMINATION – JULY- 2012		
Subj	ect o	code: 710412N Date: 11/07/20	12	
Subj	ect l	Name: Digital VLSI Design		
Time	: 2:	30 pm – 05:00 pm Total Marks:	70	
Instr	uct	ions:		
	1.	Attempt all questions.		
	2.	Make suitable assumptions wherever necessary.		
	3.	Figures to the right indicate full marks.		
0.1	4.	Draw necessary neat sketch wherever necessary.		
Q.1	(a)	Explain following process for VLSI fabrication with figures.	07	
	(b)	(i) Oxidation (ii) Photonihography Discuss the each three domain of \mathbf{Y}_{c} chart in detail	07	
	(0)	Discuss the each three domain of 1-chart in detail.	07	
Q.2	(a)	Describe important criteria to maintain design quality of VLSI.	07	
	(b)	Explain flat-band voltage in terms of MOS structure with necessary energy	07	
		band diagrams.		
		OR		
	(b)	What is threshold voltage of MOS transistor. Describe the four physical	07	
		component of threshold voltage.		
0.3	(8)	Describe Accumulation Depletion and Inversion process for the MOS	07	
X ¹⁰	(4)	system under external bias. Also derive the equation for maximum depletion	0.	
		region depth at the onset of surface inversion.		
	(b)	Write short note on voltage Boot-strapping circuit.	07	
		OR		
Q.3	(a)	Derive the equation of Drain current (I_D) for an N-channel MOSFET	07	
		operating in a linear region. Draw the necessary sketch.		
	(b)	CMOS Transmission gate (A short note).	07	
04	(a)	Even a solution lead investor with $V = 5V = l^2 - 20 \times A N^2 = V = 0.00 V D$	07	
Q.4	(a)	For a resistive load inverter with $v_{DD} = 5v$, $k_n = 20\mu A/v$, $v_{T0} = 0.8v$, $R_L = 200MO$	07	
		200 KΩ, and W/L = 2, Calculate the critical voltages on VTC and draw.		
	(h)	What is clock skew problem for NP-Domino CMOS Logic circuits Explain	07	
	(0)	True Single Phase Clock (TSPC) Dynamic CMOS Logic circuits.	07	
		OR		
Q.4	(a)	Derive the switching threshold (V_{th}) for CMOS inverter. Also prove that for	07	
		$(W) \sim (W)$		
		symmetric inverter $\left(\frac{-L}{L}\right) \approx 2.5 \left(\frac{-L}{L}\right)$.		
	(h)	Write a short note on Pre-discharge and Evaluate logic for dynamic logic	07	
	(0)	circuits.	07	
Q.5	(a)	Explain N-well process.	07	
-	(b)	Short note on FPGA.	07	
		OR		
Q.5	(a)	Define delay time definitions for a CMOS inverter.	07	
	(b)	Short note on CPLD.	07	