Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

M.E –Ist SEMESTER–EXAMINATION – JULY- 2012

Subject code: 714103N **Date: 09/07/2012**

Subject Name: Digital Signal Processor Architecture

Time: 2:30 pm – 05:00 pm **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1 **(a)** Let the analog signal be represented as **07**

$$x(t) = 3\cos(50\pi t) + 2\sin(300\pi t) - 4\cos(100\pi t)$$

What is the Nyquist rate for this signal? If the signal is sampled with sampling frequency of 200 Hz, what will be the discrete-time signal obtained after sampling? What will be the recovered signal?

(b) What is a circular buffer? Explain circular addressing mode using suitable example. State the parameters needed to handle circular buffer. **07**

Q.2 **(a)** List major hardware units of programmable digital signal processor. Briefly explain any one of them. **07**

(b) Consider a real-time DSP system running a FIR system on a 225 MHz C6713 processor at a sampling frequency of 44.1 kHz. It is known that ISR is taking 5700 cycles to perform necessary processing. Show that ISR is not running in real time and suggest at least two ways to get this ISR run in real time. **07**

OR

(b) Consider second-order IIR system given by **07**

$$H(z) = \frac{1}{1 - 0.9z^{-1} + 0.2z^{-2}} \qquad \text{(Direct form I realization)}$$

$$H(z) = \frac{1}{\left(1 - 0.5z^{-1}\right)\left(1 - 0.4z^{-1}\right)} \qquad \text{(Cascade realization)}$$

(1) Consider quantization of coefficients for both the realizations using four bits with first bit representing the sign bit. Write expressions for quantized transfer functions for both realizations.

(2) Find out pole locations for original transfer function, quantized direct form I realization and quantized cascade realization. Which realization is more sensitive to quantization of coefficients?

Q.3 **(a)** Draw block diagram of typical DSP system and explain function of each block. **07**

(b) List and explain different performance measures of DSP system. **07**

OR

Q.3 **(a)** Explain different techniques adopted for increasing the number of memory accesses per instruction cycle. **07**

(b) Explain control hazard in pipeline. Explain how delayed branch instructions are superior to branch instructions without delay. **07**

Q.4 **(a)** List and explain different buses of TMS320C5X. **07**

(b) Explain the pipeline operation for following program. **07**

```
ADD     #2500h
SAMM    TREG0
MPY     *+
SQRA    *+, AR2
```

OR

Q.4 **(a)** Write TMS320C5X assembly language program to add four consecutive data entries from memory address 60H onwards to accumulator. **07**

(b) List various registers used with ARAU of TMS320C5X and explain their functions. **07**

Q.5 **(a)** List various functional units in 'C6X CPU and explain their functions. **07**

(b) List the components of data path for TMS320C67x. **07**

OR

Q.5 **(a)** Briefly explain VLIW processing flow for C6000 CPU. **07**

(b) Explain following instruction with suitable example: **07**

```
MVK  .S2  -0x012, B2
```

****