Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

M.E –Ist SEMESTER–EXAMINATION – JULY- 2012

Subject code: 715201N **Date: 05/07/2012**

Subject Name: Semiconductor Device Modeling

Time: 2:30 pm – 05:00 pm **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Explain the temperature dependence of the resistivity of an extrinsic semiconductor.	**07**
	(b)	What is Fermi energy level in a semiconductor? Explain the dependence of the position of the Fermi level on doping levels	**07**
Q.2	**(a)**	Draw the band diagrams of a p – n junction diode under zero bias, forward and reverse biases and explain the diagrams.	**07**
	(b)	Obtain expression for the built in voltage V_{bi} of an unbiased p – n junction diode. If the doping concentrations on both sides of the junction are $10^{16}/cm^3$, determine the built in voltage. Assume $n_i = 8.7 \times 10^9/cm^3$.	**07**
		OR	
	(b)	Prove that the Fermi level will be flat if the current through a semiconductor is zero.	**07**
Q.3	**(a)**	Draw the cross section of a bipolar junction transistor and explain the various regions. What are the relative doping concentrations of emitter, base and collector and what is the reason for this profile?	**07**
	(b)	Draw the family characteristics of common emitter and common base configurations and compare them.	**07**
		OR	
Q.3	**(a)**	Discuss the current flow through an n-p-n BJT describing the various current components and their origins.	**07**
	(b)	Define common base current gain and common emitter current gain. Discuss how they are related. Explain the reason why the common base current gain does not vary much with change in collector bias while the common emitter current gain varies much with change in the collector bias.	**07**
Q.4	**(a)**	Draw and explain the band diagrams for a MOS capacitor (diode) made on p type silicon substrate with the bias on the metal electrode varying from a negative value to a large positive value.	**07**
	(b)	Define threshold voltage for a MOS diode. What is the effect of work function differences between metal and semiconductor on the threshold voltage?	**07**
		OR	
Q.4	**(a)**	Explain the structure of an n channel enhancement MOSFET and its operation.	**07**
	(b)	Explain what is meant by channel length modulation in a MOSFET and what is the effect on the IV characteristics of a MOSFET? Give the expression for the drain current in the saturation region with channel length modulation present.	**07**

Q.5	**(a)**	What is trench isolation technique that is used in the present day CMOS processes? Explain how this structure is formed.	**07**
	(b)	Explain the terms defect density, yield and die size in VLSI technology. What is the relation between these parameters?	**07**

OR

Q.5	**(a)**	What is meant by planarization that is encountered in multilevel metal processes and what is its importance?	**07**
	(b)	What is photo resist and what is the role of photo resist in VLSI processing?	**07**

****