Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

M.E –IIst SEMESTER–EXAMINATION – JULY- 2012

Subject code: 725201 **Date: 06/07/2012**

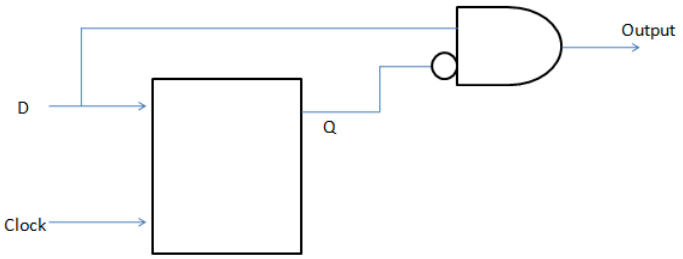
Subject Name: Digital VLSI Design II-BE

Time: 10:30 am – 13:00 pm **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Draw a diagram that illustrates a standard backend flow from synthesis to GDSII. Make sure you include testability. How would the flow change?	**07**
	(b)	What is the difference between a Wireload model & TLUplus file? When are they used and what is their importance in IC design	**07**
Q.2	**(a)**	List all the libraries / files that you use for Physical design & GLS. Write a brief note about each one of them	**07**
	(b)	What are multi-cycle paths, false paths and case-analysis in static timing?	**07**
		OR	
	(b)	In a design that violates setup time constraints, would you recommend option A or option B below? Justify? A. Increase the operating voltage B. Iterate through backend till timing is met	**07**
Q.3	**(a)**	What are the steps involved in the Floor planning stage and what is their importance?	**07**
	(b)	What is setup & hold time. How do they affect the timing of a digital circuit with any equations?	**07**
		OR	
Q.3	**(a)**	A design has been synthesized for 300MHz. However, after place and route, the results of Primetime indicate that there are timing violations. The WNS is -0.4ns and the TNS is -1.2ns. What is the frequency that this design can run at now, if we were to ignore this violation and send the design for fabrication?	**07**
	(b)	In a company there is a situation that one chip is timing critical and another chip is area critical. What are the different optimization steps you suggest in a typical design flow?	**07**
Q.4	**(a)**	In scan chains, what type of violations is more likely: setup or hold? Why? What would you do to fix them? What is the avoidance strategy?	**07**
	(b)	What is a Milkyway environment? What are the different components of it?	**07**
		OR	
Q.4	**(a)**	How do you find the max_transition violations in a design? What is the command? Once the violations are found, what is the fix?	**07**
	(b)	Describe the command import_designs with all the steps executed as a part of it with a simple example	**07**
Q.5	**(a)**	Explain the following terms **A.** Critical Path **B.** Congestion **C.** Scan Chain **D.** Stuck at Fault	**07**
	(b)	Describe the behavior of the circuit for 0111100011 input sequence with timing diagram and derive any name for the circuit	**07**



OR

Q.5	**(a)**	Explain the following terms **A.**TNS **B.** WNS **C.** PVT Conditions **D.** Clock Uncertainty and Jitter	**07**
	(b)	What is the difference between a wire delay and cell delay? How do they affect the timing of the digital circuit?	**07**

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