Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

M.E-III[rd] SEMESTER–EXAMINATION – MAY- 2012

Subject code: 732604 Date: 10/05/2012

Subject Name: Low Power CMOS VLSI Circuit Design

Time: 10:30 am – 01:00 pm Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	What is the significance of Switching Activity Reduction? Explain various technique used for the same in order to reduce power dissipation.	**07**
	(b)	Explain the source of power dissipation responsible for failure in VLSI Circuit.	**07**
Q.2	**(a)**	Discuss the significance of Low Power Design in VLSI? Explain dynamic power dissipation.	**07**
	(b)	The Chip size of a CPU is 15 mm x 25mm with clock frequency of 300MHz operating at 3.3V. The length of the clock routing is estimated to be twice the circumference of the chip. Assume that the clock signal is routed on a metal layer with width of 1.2 µm and the parasitic capacitance of the metal layer is 1fF/µm^2. What is the power dissipation of the clock signal?	**07**
		OR	
	(b)	Explain Low Power Circuit Technique: Self-Reverse Biasing and Multi-V_T Technique.	**07**
Q.3	**(a)**	Compare Wooley Multiplier and Booth Multiplier.	**07**
	(b)	Explain the BiCMOS Adder.	**07**
		OR	
Q.3	**(a)**	Explain Current-Mode Adders.	**07**
	(b)	Discuss in detail the operation of Sense Amplifier.	**07**
Q.4	**(a)**	Discuss Data Retention Power Sources for DRAM and SRAM.	**07**
	(b)	Explain Low Power ROM Technology and Briefly discussed the future trend and development of ROM	**07**
		OR	
Q.4	**(a)**	Discuss in detail Self-Refresh Circuit of DRAM.	**07**
	(b)	Explain Half Voltage Generator (HVG) and Back Bias Generator (BVG).	**07**
Q.5	**(a)**	Explain Parallel and Pipelining architecture methodology used for low power VLSI design.	**07**
	(b)	Discuss various sources of power dissipation in DRAM and SRAM.	**07**
		OR	
Q.5	**(a)**	Discuss the Low-Power Clocking.	**07**
	(b)	Discuss the various implementation options for Low Power.	**07**

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