Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

M.E -IVth SEMESTER–EXAMINATION – MAY- 2012

Subject code: 740301 **Date: 12/05/2012**

Subject Name: Advanced VLSI Design

Time: 02:30 pm – 05:00 pm **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Explain Register Balancing for timing in Architecting Speed.	**07**
	(b)	Explain impact of Resources Without Set on Area.	**07**
Q.2	**(a)**	Explain gated clocks in ASIC prototypes.	**07**
	(b)	Explain Pipelining, retiming, and register balancing for performance optimization.	**07**
		OR	
	(b)	Explain the dangers of the “parallel_case” and “full_case” directives.	**07**
Q.3	**(a)**	Explain issues related to software/hardware code sign.	**07**
	(b)	Explain Low-latency architectures for minimizing the delay from the input of a module to the output.	**07**
		OR	
Q.3		Explain problems introduced by fully synchronized resets and how it can be solved.	**14**
Q.4	**(a)**	Explain Combinatorial loops versus sequential loops.	**07**
	(b)	Explain Graphical State machines in brief.	**07**
		OR	
Q.4	**(a)**	Define Metastability. Expalin any two solution of metastability problem.	**07**
	(b)	Explain the impact of clock control on dynamic power consumption.	**07**
Q.5		Explain all partitioning methods in design organization.	**14**
		OR	
Q.5	**(a)**	Explain how resets can be managed over multiple clock domains.	**07**
	(b)	Explain potential hazard on reset pin, and draw waveform with reset hazard in internally generated reset.	**07**

****