Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

ME – SEMESTER-1 (NEW) EXAMINATION – WINTER 2016

Subject Code: 2710507 **Date:04/01/2017**

Subject Name: ASIC DESIGN

Time: 2:30 pm to 5:00 pm **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Draw and Explain FPGA Architecture	**07**
	(b)	What is VHDL? List major capabilities of VHDL along with the features that differentiate it from other hardware description languages	**07**
Q.2	**(a)**	Briefly explain Finite State Machine (FSM). Compare Moore and Mealy state machine.	**07**
	(b)	Explain basic data types in VHDL.	**07**
		OR	
	(b)	Explain following statement with example (1) when….else (2) with…select	**07**
Q.3	**(a)**	Write a VHDL code for 4 X 1 multiplexer using dataflow and behavioral modeling.	**07**
	(b)	Write the VHDL code for JK Flip-flop. Consider preset and clear as direct inputs.	**07**
		OR	
Q.3	**(a)**	Write a VHDL program for 4 bit binary parallel adder using structural modeling. Use full adder as component.	**07**
	(b)	Explain ASIC Design flow with diagram.	**07**
Q.4	**(a)**	Explain following statements (1) Exit Statement (2) Process Statement (3) Generate Statement	**07**
	(b)	Explain wait statement with different clauses.	**07**
		OR	
Q.4	**(a)**	What do you mean by Delta-delay? Also explain Inertial Delay model and Transport Delay model.	**07**
	(b)	Explain configuration and package declaration statements using necessary examples	**07**
Q.5	**(a)**	Using case – when statements write VHDL listing for 3X8 Decoder with enable and reset signal facility	**07**
	(b)	Write VHDL code for 1011 sequence detector using FSM.	**07**
		OR	
Q.5	**(a)**	Describe architecture of PAL and PLA, compare and contrast advantages and disadvantages over each other.	**07**
	(b)	Describe CPLD architecture and explain how it can be programmed.	**07**

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