Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

ME – SEMESTER-1 (NEW) EXAMINATION – WINTER 2016

Subject Code: 2712602 **Date:04/01/2017**

Subject Name: CMOS CIRCUIT DESIGN-I

Time: 2:30 pm to 5:00 pm **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	List complete classification of CMOS Op-Amps and explain Two Stage CMOS Op-Amp in brief.	**07**
	(b)	Derive voltage gain Av, output resistance Rout and 3-db Bandwidth equations for Source follower.	**07**
Q.2	**(a)**	Draw 4x4 bit array multiplier for unsigned numbers and discuss it in brief.	**07**
	(b)	Explain need of transistor matching in case of current mirror and discuss different layout techniques.	**07**
		OR	
	(b)	Explain in brief an intuitive method of small signal analysis.	**07**
Q.3	**(a)**	Explain Miller Compensation for CMOS Op-Amp.	**07**
	(b)	Discuss in brief Sense Amplifier.	**07**
		OR	
Q.3	**(a)**	Derive $I_{D(Sat)}$ and $I_{D(Lin)}$ for n channel MOSFET.	**07**
	(b)	Discuss in brief Mixed Signal VLSI issues in CMOS Technologies.	**07**
Q.4	**(a)**	Explain in detail Wilson Current Mirror.	**07**
	(b)	Discuss Linear Carry Select Adder for 4 bit as well as 16 bit. Also show critical path in gray shad in 16 bit adder block diagram.	**07**
		OR	
Q.4	**(a)**	Discuss Cascode Current Mirrors.	**07**
	(b)	Define the following with respect to Differential Amplifier. (i) CMRR (ii) ICMR (iii) Output Offset Voltage (iv) PSRR (v) Differential Mode Voltage (vi) Common Mode Voltage (vii) Slew Rate.	**07**
Q.5	**(a)**	Discuss Barrel shifter and logarithmic shifter in brief.	**07**
	(b)	Discuss Gilbert cell and voltage headroom.	**07**
		OR	
Q.5	**(a)**	Explain in brief second order effects.	**07**
	(b)	Explain in detail power consumption in CMOS Gates. Discuss Static & Dynamic power dissipation in CMOS Circuits.	**07**

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