Seat No.: _____ Enrolment No._____

# GUJARAT TECHNOLOGICAL UNIVERSITY

**ME – SEMESTER-1 (NEW) EXAMINATION – WINTER 2016**

**Subject Code: 2712605 Date:05/01/2017**

**Subject Name: Physics of MOS Transistor**

**Time: 2:30 pm to 5:00 pm Total Marks: 70**

**Instructions:**

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

**Q.1** **(a)** Identify the region (ON/OFF and linear/saturation) of operation for MOSFET device for the cases given below: **07**

a. N-channel MOSFET with $V_T = 2$ V; $V_G = 5$ V, $V_B = 0$ V, $V_D = 0$ V, and $V_S = 0$ V.

b. N-channel MOSFET with $V_T = 2$ V; $V_G = 5$ V, $V_B = 0$ V, $V_D = 4$ V, and $V_S = 0$ V.

Draw cross section of n-channel MOSFET and indicate inversion layer in each of the above two cases.

**(b)** Draw $I_{DS}$ versus $V_{GS}$ characteristics on a liner as well as log scale for n-channel MOSFET for three different values of $V_{BS}$ (i. e. $V_{BS3} < V_{BS2} < V_{BS1} = 0$ V) for a $V_{DS} = V_{DD}$. **07**

**Q.2** **(a)** Define various capacitances in MOS capacitor system and obtain exact expressions for $C'_b$ and $C'_i$. **07**

**(b)** Derive approximate expressions for inversion charge and surface potential for MOS capacitor operating in weak inversion region. Define parameter *n*. **07**

**OR**

**(b)** Draw p-type substrate two terminal MOS structure and its band diagram for three different region of operation; 1. Flat-band, 2. Accumulation and 3. Depletion and inversion. **07**

**Q.3** **(a)** Explain how the splitting of Fermi level takes place in three-terminal p-substrate MOS structure when $V_{CB}$ is negatively increased from a level of 0. Draw necessary energy band diagram. Obtain expression for electron concentration at the surface for this p-type substrate three-terminal MOS structure. **07**

**(b)** Derive accurate strong inversion model (basis of level 2 model in Berkeley Spice Simulator) for four-terminal p-type substrate MOS structure. **07**

**OR**

**Q.3** **(a)** Plot surface potential as a function of $V_{CB}$ for different values of $V_{GB}$. Obtain expressions for following important $V_{CB}$ values: $V_Q$, $V_W$, and $V_U$. **07**

**(b)** Derive the strong inversion drain current model which is the basis of "level 3" model implemented in Berkely Spice simulator. **07**

**Q.4** **(a)** Define α parameter used in simplified charge sheet model. Discuss the effect of α parameter on the accuracy of simplified strong inversion model. **07**

**(b)** Define drain-induced barrier lowering. Derive the expression for the drop in threshold voltage in short-channel MOSFET device compared to long-channel device for deep source/drain regions. **07**

**OR**

**Q.4** **(a)** Discuss following for MOSFET device: 1. Various scattering phenomena and their effect on mobility, and 2. Effect of increasing temperature on mobility and leakage current. **07**

**(b)** Discuss the effect of using shallow-trench isolation technique on narrow channel effect along with mathematical analysis. Briefly compare the above effect with that in case of using LOCOS technique. **07**

**Q.5** **(a)** Discuss different components of source/drain resistance and derive expression for $I_{DS}$ taking into account effects of source/drain resistance. **07**

**(b)** What do you understand by non-quasi-static effect? Explain non-quasi-static effect with a simple circuit of NMOS applied with a fixed drain voltage and a pulse excitation at the gate terminal. **07**

**OR**

**Q.5** **(a)** Show that due to velocity saturation effect, the drain current in short-channel MOSFET does not follow square-law. Also justify that the required ratio of (W/L) of PMOS and NMOS devices is less than 2 for equal driving capability in short-channel devices. **07**

**(b)** What are the different benchmark tests to evaluate MOSFET models? What should be the behavior of $I_D$, Q, and capacitances model equations at $V_{DS}$ = 0 V? Draw the test setup to verify the same. **07**

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