Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

ME – SEMESTER-1 (NEW) EXAMINATION – WINTER 2016

Subject Code: 2715410 **Date:06/01/2017**

Subject Name: Advanced Digital Circuit Design

Time: 2:30 pm to 5:00 pm **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Explain in detail bocking and non blocking statement with example	**07**
	(b)	What is the difference between Moore and Mealy finite state machines? Write Verilog code for Traffic light controller.	**07**
Q.2	**(a)**	Write the Verilog Description for 4 x 1 multiplexer using Gate level modelling	**07**
	(b)	Briefly discuss the different ways of the timing control in Verilog.	**07**
		OR	
	(b)	Explain in detail different variable data type in Verilog.	**07**
Q.3	**(a)**	Write a verilog code for Mod 9 counter	**07**
	(b)	Give the points of difference between tasks and function Explain with suitable example.	**07**
		OR	
Q.3	**(a)**	Write a verilog code for a ring counter.	**07**
	(b)	Write the Verilog code to implement Digital clock	**07**
Q.4	**(a)**	Write the Verilog code to implement ALU with given specification. There are two data each of 4 bits and two bits control line If control is ‘00’ must do addition,’01’ substraction,’10’ multiplication,’11’ division Assume data is available parallel	**07**
	(b)	Write a Verilog code to detect the sequence “0110”	**07**
		OR	
Q.4	**(a)**	What is Multi Level Logic Minimization? Explain in detail Global Optimization Technique	**07**
	(b)	Explain with neat diagram IOB(Input Output Block) of FPGA	**07**
Q.5	**(a)**	What are the draw back of K-L Algorithm and how they are rectified in Extension of K-L Algorithm	**07**
	(b)	Explain in detail Iterative-improvement algorithm for Partitioning	**07**
		OR	
Q.5	**(a)**	Explain Timber wolf placement algorithms based on simulated annealing	**07**
	(b)	Discuss difference between modules and module instances.	**07**

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