Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

ME – SEMESTER II– EXAMINATION – WINTER - 2016

Subject Code: 2722602 Date: 17/11/ 2016

Subject Name: CMOS Circuit Design - II

Time: 2:30 pm to 5:00 pm Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks**

Q.1 **(a)** Show that the charge injection in NMOS/PMOS switch results into non-unity gain, dc offset, and non-linearity in V_{out} as a function of V_{in}. Explain the trade-off between charge injection and speed of the switch. **07**

(b) Draw switched-capacitor (SC) unity gain buffer circuit which has three switches. What should be the sequence of operation of switches to minimize the error? Justify your answer. Derive expression for precision of this circuit. **07**

Q.2 **(a)** In a self-bias voltage reference circuit with resistor biasing, derive the dependence of output current on output resistance of each transistor in the circuit. **07**

(b) Show with appropriate reference generator circuit that the output noise is approximately same as input-referred noise voltage of op amp. **07**

OR

(b) How can we achieve temperature-independent output voltage in voltage reference circuit? Explain the principle of operation in detail with necessary derivation. Show that if one voltage source is taken as V_{BE}, then second voltage source should be 17.2 V_T. **07**

Q.3 **(a)** Derive transfer function of simple PLL and discuss trade-off between various parameters to improve its performance. **07**

(b) What will be the effect of unequal charging and discharging current in basic charge pump PLL on its operation? Explain with necessary waveforms. **07**

OR

Q.3 **(a)** Explain with necessary diagrams and waveforms the issue observed in basic charge pump PLL due to finite capacitance seen at the drains of current sources. Suggest possible solution to this problem. **07**

(b) Explain the effect of dead zone in charge pump circuit. How can you avoid it? Explain with necessary waveforms. **07**

Q.4 **(a)** Compare open-array and folded-array organization architectures of memory chip. Draw necessary schematics for both of them. **07**

(b) Explain the basic concept of using DSM (delta-sigma modulation) in sensing a flash memory. **07**

OR

Q.4 **(a)** Sketch and explain a circuit for sensing resistive memory using a concept of DSM and derive expression of R_{mbit}. **07**

(b) Draw cross section of floating memory element and explain its operation from the point of view of reading, writing and erasing. **07**

Q.5	**(a)**	Draw and explain the block diagram of voltage comparator. Discuss the operation of positive feedback decision circuit with necessary equations in detail.	**07**
	(b)	Derive noise figure expression for common-source stage LNA having resistive feedback.	**07**

OR

Q.5	**(a)**	Draw block diagram of dual slope ADC and explain its operation with necessary mathematical analysis.	**07**
	(b)	List out various LNA topologies. Explain quantitatively operation of common source stage with inductive load LNA along with diagram.	**07**

****