Date: 21/11/2016

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GUJARAT TECHNOLOGICAL UNIVERSITY

ME – SEMESTER II– EXAMINATION – WINTER - 2016

Subject Code: 2722606

Subject Name: Algorithms for VLSI Physical Design Automation Time: 2:30 pm to 5:00 pm Total Marks: 70

Instructions:

- 1. Attempt all questions.
- 2. Make suitable assumptions wherever necessary.
- 3. Figures to the right indicate full marks

Q.1 (a) Do as Directed:

- (i) Discuss advantage of building-block design style.
- (ii) How to deal with K-way partition using Kernighan-Lin Algorithm?
- (iii) Draw and explain Channel intersection graph.
- (iv) Discuss semi perimeter method to explain Maze routers.
- (v) Discuss need of Dogleg Algorithm
- (vi) Explain Structural level layout generation
- (vii) Discuss crossover in genetic Algorithm

(b) Apply Fiduccia Mattheyses (FM) algorithm to partition following circuit: 07



Q.2	(a)	Discuss Polar and Adjacency graphs in Floorplan.	07
	(b)	Compare Kernighan-Lin and Fiduccia-Mattheyses heuristics in reference to circuit partitioning problem	07
		OR	
	(b)	Discuss optimization of Gate-matrix Layout.	07
Q.3	(a) (b)	Discuss Cluster growth algorithm for Floor planning in brief. Explain Soukup's Algorithm.	07 07
		OR	
Q.3	(a) (b)	Draw and explain Gate array Layout. Explain min-cut placement algorithm along with its limitations.	07 07
Q.4	(a) (b)	Explain Genetic Algorithm in brief. Discuss Integer Programming for global routing.	07 07
		OR	
Q.4	(a) (b)	Discuss basic left-edge algorithm Discuss simulated annealing algorithm for Floor planning in brief.	07 07
Q.5	(a)	Compare Lee algorithm and Line search algorithm. Discuss Mikami- Tabuchi's Algorithm.	07
	(b)	Discuss the problem of minimizing the layout of a PLA.	07
		OR	-
Q.5	(a)	Elaborate design steps in VLSI design process. What are the difficulties associated with physical design?	07
	(b)	Explain in brief:	07
		1. List the possible criteria to measure quality of floorplan.	
		2. Discuss factors which decide cost function for placement algorithm.	
