Seat No.: _____ **Enrolment No._____**

GUJARAT TECHNOLOGICAL UNIVERSITY

M. E. - SEMESTER – II • EXAMINATION – WINTER • 2016

Subject code: 2724204 **Date: 21-11-2016**

Subject Name: HDL BASED DESIGN WITH PROGRAMMABLE LOGIC

Time: 02:30 pm - 05:00 pm **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1 (a) Do as Directed. 07

1. What is the difference between a Transaction and an Event?
2. What is the priority level of different branches in the CASE statement?
3. Process statement can be used to describe sequential logic only. Justify whether the statement is True or False?
4. Declare a memory data type of 8 registers with size of each register 32 bits.
5. Write a VHDL statement to model a 3 i/p NAND gate with inertial delay of 5 ns?
6. What is the difference between the types STD_LOGIC and STD_ULOGIC?
7. What does VHDL stands for?

(b) Explain various types of delays in VHDL. 07

Q.2 (a) Compare merits and demerits of full custom versus semicustom design style. 07

(b) Draw and discuss the architecture of FPGA. 07

OR

(b) Draw and discuss the architecture of CPLD 07

Q.3 (a) Define Event-Driven Simulator and Cycle Based Simulator. Discuss the operation of Cycle Based Simulator with suitable example. 07

(b) Implement below given Boolean logic functions using the ROM of suitable size. 07

F0 = A' B' C + A B' C' + A B' C F2 = A' B' C' + A' B' C + A B' C'

F1 = A' B' C + A' B C' + A B C F3 = A' B C + A B' C' + A B C'

OR

Q.3 (a) Develop the PLA table to implement below given Boolean equations using PLA. 07

F0 = A + B' C' F2 = B' C' + A B

F1 = A C' + A B F3 = B' C + A

(b) What are the various abstraction levels of VLSI design? Explain any two of them in detail. 07

Q.4 (a) Mention the parameters responsible for the selection of the FPGA device for a given application. Write a VHDL code for 4x1 MUX. 07

(b) Write the VHDL description for a decade counter using FSM design style. 07

OR

Q.4 (a) What is the difference between a D Flip Flop and a D Latch? Write the VHDL code for both. 07

(b) Answer the questions based on the analysis of the given VHDL code. 07

```
-----------------------------------
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_unsigned.all;
use ieee.std_logic_arith.all;
-----------------------------------
entity PQR is
port(   A: in std_logic_vector(1 downto 0);
        B: in std_logic_vector(1 downto 0);
        Sel: in std_logic_vector(1 downto 0);
        Res: out std_logic_vector(1 downto 0)
);
end PQR;
-----------------------------------
architecture XYZ of PQR is
begin

    process(A,B,Sel)
    begin

        -- use case statement to achieve
        -- different operations of PQR

        case Sel is
            when "00" =>
                Res <= A + B;
            when "01"
=>

                Res <= A + (not B) + 1;
            when "10" =>
                Res <= A and B;
            when "11" =>
                Res <= A or B;
            when others =>
                Res <= "XX";
        end case;
    end process;
end XYZ;
-------------------------------------------
```

1. List the libraries used in the given sample code.
2. What is the functionality implemented?
3. Implemented digital logic circuit is Combinational or Sequential?
4. What is the size of the datapath?
5. Which design style is used in the given code, Structural, Behavioural or Dataflow?
6. What is the name of the entity?
7. What is the role of following statement?

```
when others => Res <= "XX";
```

Q.5 (a) Discuss with example various types of modelling styles supported in VHDL. 07

(b) What is HDL? Discuss the relative differences between two widely used HDLs - VHDL and Verilog. 07

OR

Q.5 (a) Explain following VHDL constructs. 07

1. Guarded Block Statement
2. CASE Statement

(b) Differentiate the Modelling for Synthesis vs. Modelling for Simulation in HDL based design. 07