Seat No.: _____ **Enrolment No._____**

GUJARAT TECHNOLOGICAL UNIVERSITY

M. E. - SEMESTER – II • EXAMINATION – WINTER • 2016

Subject code: 2724209 **Date: 19-11-2016**

Subject Name: VLSI Signal Processing

Time: 02:30 pm - 05:00 pm **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1 (a) Define Following terms in reference to VLSI Signal Processing. 07

1. Iteration
2. Iteration Period
3. Loop Bound
4. Critical Loop
5. Cutset
6. Critical Path
7. Feed Forward Cutset

(b) Derive the expression for clock period in wave pipelining. 07

Q.2 (a) Prove that Unfolding preserves the number of delays in a DFG. 07

(b) Compute iteration bound of the system, represented by DFG given in Figure 1 using LPM technique. 07

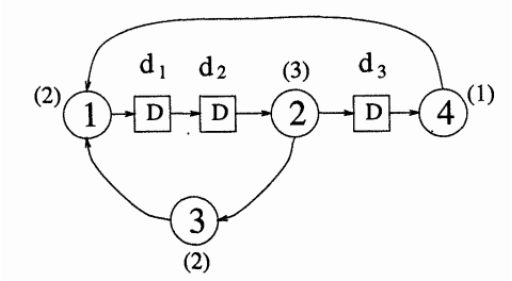

Figure 1

OR

(b) Why use Parallel Processing when Pipeline Processing can be used equally well? Briefly explain with example. 07

Q.3 (a) Discuss Redundant Number Representation. 07

(b) Compare Pipelining & Parallel Processing for VSP. 07

OR

Q.3 (a) Discuss Data Format Conversion. 07

(b) Explain in detail pipeline concept used in sequential circuits. 07

Q.4 (a) Explain Fast Convolution. 07

(b) What is the need for systolic architecture design? Discuss systolic architecture design in detail. 07

OR

Q.4	(a)	Define systolic design methodology. Compare it with other design methodologies.	07
	(b)	Briefly explain the algorithm of unfolding.	07
Q.5	(a)	Write a note on Wave Pipelining.	07
	(b)	Discuss Multiple Constant Multiplications.	07

OR

Q.5	(a)	Discuss Power Reduction Techniques.	07
	(b)	Apply the unfolding technique to DSP algorithm given in Figure 2 with unfolding factor equal to 4.	07

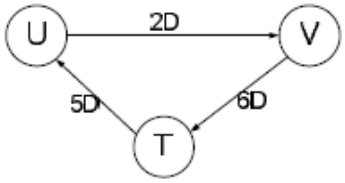

Figure 2