Seat No.:	Enrolment No
-----------	--------------

## GUJARAT TECHNOLOGICAL UNIVERSITY

ME - SEMESTER III (NEW) - EXAMINATION - WINTER-2016

Subject Code: 2732605 Date:25/10/2016 **Subject Name: VLSI Test Principles and Architectures** Time: 02:30 pm to 05:00 pm **Total Marks: 70 Instructions:** 1. Attempt all questions. 2. Make suitable assumptions wherever necessary. 3. Figures to the right indicate full marks. 07 Q.1 Define or briefly explain following terms: 1. Rule of Ten, 2. Yield, 3.Error, 4. (a) Design for testability, 5. Fault, 6. Transient power supply testing, and 7. Fault collapsing Explain various bridging fault models. **07 (b)** Draw and explain Enhanced Scan Architecture. 07 0.2 (a) Discuss SCOAP based testability analysis and determine SCOAP combinational **07 (b)** measures for 3 input OR gate. OR Draw Edge triggered muxed D scan cell design and explain its operation with **07 (b)** help of waveforms. Explain parallel pattern fault simulation (PPFS) with the help of an example. **Q.3** (a) **07** Discuss transport delay model and inertial delay model concept for timing delay **(b) 07** models. OR **Q.3** (a) What is Hazard? Explain various types of hazards. **07** Explain any two techniques for Logic element evaluation. **07 (b)** Discuss D-algorithm which is used to generate vectors in combinational circuits **Q.4** 07 (a) (No need to give Pseudo code). **(b)** How Genetic algorithm is used for ATPG? Explain in detail. **07** OR 0.4 With an example, explain the concept of Boolean difference. **07** (a) Explain the concept of time frame expansion in sequential ATPG. **07 (b) Q.5** Explain parallel signature analysis output response compaction technique. 07 (a) **(b)** What is the importance of Cellular Automata in Pseudo-Random Testing? **07** Explain in detail. OR Explain the single capture clocking scheme to test multiple clock domain. **Q.5 07** (a) **(b)** How you will enhance the fault coverage? Write down three approaches for **07** that in brief.

\*\*\*\*\*\*