Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

ME – SEMESTER III (NEW) – EXAMINATION – WINTER-2016

Subject Code: 2734203 **Date:25/10/2016**

Subject Name: HIGH SPEED CMOS VLSI CIRCUIT

Time:02:30 pm to 05:00 pm **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	(a)	Explain Dielectric Thickness and Permittivity with respect to Process Variation?	07
	(b)	Explain the Complex model use for calculus of the delay in MOS circuits.	07
Q.2	(a)	Explain the Static CMOS.	07
	(b)	Explain inter die variations.	07
		OR	
	(b)	What is the importance of latching? Explain the performance of latching circuit with different mechanisms.	07
Q.3	(a)	What is Mathematic Optimization? Compare different optimization algorithms.	07
	(b)	Explain Static and Dynamic Latches.	07
		OR	
Q.3	(a)	Write a short note on the working of Pseudo Inverter latch.	07
	(b)	What are the different Causes which fail the functionality of Chip?	07
Q.4	(a)	Explain the Non-clocked Logic Circuit.	07
	(b)	What are the problems in controlling precharge circuit with single clock? Explain Cross Coupled Differential Output.	07
		OR	
Q.4	(a)	Explain the use of CAD Toll for Optimization.	07
	(b)	Write short note on the Latch Domino Logic.	07
Q.5	(a)	What is Circuit Optimization? Explain the different Types of Circuit Optimization.	07
	(b)	Explain the Dynamic Pass Transistor Circuit.	07
		OR	
Q.5	(a)	What are the different process variations to take care for optimization of VLSI Circuit?	07
	(b)	Explain Channel Width Effect Cause because of Process Variation?	07