Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

ME – SEMESTER IV (NEW) – • EXAMINATION – WINTER 2016

Subject Code: 2745402 Date: 26/10/2016

Subject Name: CORTEX-M4 PROCESSOR ARCHITECTURE AND PROGRAMMING

Time:02:30 pm to 05:00 pm Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

			MARKS
Q.1		**Short Questions**	**14**
	1	What is the use of Q bit in XPSR register?	
	2	What is a bit banding technique?	
	3	What is a SYSTIC timer?	
	4	Explain the use of branch Prediction in pipeline?	
	5	How do you select specific CORTEX-M series Processor?	
	6	Give advantage of unaligned memory accesses compare to ARM Processor.	
	7	If the pipeline is wider, the instruction throughout is high-True/False?	
	8	Explain CPS instruction.	
	9	What is the use of PDDS bit in power control register?	
	10	How to Enable FPU exception interrupts?	
	11	How NVIC exception entry and exit occur?	
	12	What are the types of Cortex-M series?	
	13	Which three things need to use NVIC?	
	14	Explain DSB instruction with example.	
Q.2	**(a)**	Explain Pre-indexed addressing and Post-indexed addressing.	**03**
	(b)	Explain the CPU Operating Modes.	**04**
	(c)	Discuss the differences between ARM architecture and CORTEX architecture. Describe the merits and demerits also.	**07**
		OR	
	(c)	Explain in Detail Cortex-M family Processor Architecture.	**07**
Q.3	**(a)**	Explain the XPSR register.	**03**
	(b)	Explain 1) SADD 2) SHADD with Example.	**04**
	c)	Explain Application Program Status register.	**07**
		OR	
Q.3	**(a)**	Explain the CMSIS usage and benefits.	**03**
	(b)	Explain CMSIS Register Core.	**04**
	c)	Explain the memory map with diagram.	**07**
Q.4	**(a)**	What is Bus Interface Unit? Enlist types of Bus Interface Unit?	**03**
	(b)	Explain the low power modes of cortex.	**04**
	(c)	Explain with block diagram of Cortex Microcontroller Software Interface standard (CMSIS).	**07**
		OR	
Q.4	**(a)**	Explain QADD and QSUB instruction.	**03**
	(b)	Explain Reset of Cortex.	**04**

	c)	Explain the Programmer's model of cortex.	**07**
Q.5	**(a)**	Explain Debug architecture and interfaces.	**07**
	(b)	What is the difference between THUMB 1 and THUMB2 Architecture?	**07**
		OR	
	(a)	Explain Debug Modes.	**07**
	(b)	How branch instructions are executed in CORTEX M4?	**07**

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