Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

ME – SEMESTER-1 (NEW) EXAMINATION – WINTER 2016

Subject Code: 3715204 **Date:07/01/2017**

Subject Name: Digital VLSI Design & Verification - I Frontend

Time: 2:30 pm to 5:00 pm **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	What is static timing analysis? Explain the difference between STA and DTA?	**07**
	(b)	What is test bench? Explain with example?	**07**
Q.2	**(a)**	What is metastability? When/why it will occur? Explain the different ways to avoid?	**07**
	(b)	What is the difference between synthesizable and non-synthesizable IP cores? How do Synthesis tools treat the non-synthesizable IP cores?	**07**
		OR	
	(b)	Draw the layout for the below Boolean equations a) Y=~(a+bc) b) Y=~(ab+cd)	**07**
Q.3	**(a)**	What are registered outputs? What is the impact of registered outputs on timing performance of the circuit?	**07**
	(b)	What is physical synthesis? In what way, physical synthesis gives better results?	**07**
		OR	
Q.3	**(a)**	Design full adder using 4 to 1 multiplexer and write the Verilog code for full adder.	**07**
	(b)	Write short note on soft cores, Firm cores and hard cores.	**07**
Q.4	**(a)**	What do you understand by noise margin? Draw the voltage transfer characteristic of an inverter and clearly show VIH, VIL, VOH, and VOL and write the equation for NM_H and NM_L.	**07**
	(b)	Design a state machine to detect the sequence 11011 with overlapping and non-overlapping sequence.	**07**
		OR	
Q.4	**(a)**	Explain the design of FIFO with the help of block diagram, assume that you are using FIFO in between two clock domains of different frequency.	**07**
	(b)	What is verification? Explain the difference between direct testing and constrained random verification.	**07**
Q.5	**(a)**	Design JK flip flop to D flip flop conversion?	**07**
	(b)	Write short note on a)Full custom design b)standard cell based and gate array based design	**07**
		OR	
Q.5	**(a)**	What is FSM? Design FSM to detect the sequence 1011.	**07**
	(b)	Write short note on a) NRE cost and recurring cost. b) Yield and technology scaling.	**07**

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