

Seat No.: \_\_\_\_\_

Enrolment No. \_\_\_\_\_

**GUJARAT TECHNOLOGICAL UNIVERSITY**  
**ME – SEMESTER III (NEW) – EXAMINATION – WINTER-2016**

**Subject Code: 3735203**

**Date: 25/10/2016**

**Subject Name: Verification Methodology**

**Time: 02:30 pm to 05:00 pm**

**Total Marks: 70**

**Instructions:**

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

- Q.1** (a) Explain the layered testbench in System Verilog. **07**  
(b) What is polymorphism in OOP? Explain with example. **07**
- Q.2** (a) What are assertions? What is the advantage of assertions? Explain concurrent assertion layers. **07**  
(b) Write the assertions in System Verilog for the dual-port RAM. **07**
- OR**
- (b) Explain interface in system Verilog with example. **07**
- Q.3** (a) Explain UVM simulation phases in detail. **07**  
(b) Explain different TLM ports in detail. **07**
- OR**
- Q.3** (a) Explain the UVM verification environment with example. **07**  
(b) What is UVM Factory? Why and how to register in Factory? Explain Factory override methods with syntax. **07**
- Q.4** (a) Briefly explain the Low Power Design and Verification flow. **07**  
(b) What is UPF? Explain how to create power distribution network in UPF. **07**
- OR**
- Q.4** (a) Explain in detail assertions checking in low power simulation. **07**  
(b) Explain APB slave operation in detail. **07**
- Q.5** (a) Explain different power reduction techniques in detail. **07**  
(b) Explain the need of power aware simulation in detail. **07**
- OR**
- Q.5** (a) Write a Perl script to generate the random number between 1 to 100. **07**  
(b) Write a note on Make file. **07**

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