Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

ME – SEMESTER III (OLD) – EXAMINATION – WINTER-2016

Subject Code: 730303 **Date:27/10/2016**

Subject Name: VLSI Design

Time:02:30 pm to 05:00 pm **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Explain in detail different configuration modes of FPGA.	**07**
	(b)	Explain in detail different operator types in verilog.	**07**
Q.2	**(a)**	Explain blocking and non-blocking assignments in verilog with examples.	**07**
	(b)	Explain the use of casex, casez in verilog with example.	**07**
		OR	
	(b)	Explain functions of digital clock managers in regards to Spartan 3e.	**07**
Q.3		With the help of T-flipflop design a counter that gives 1,4,3,6,9,2,0…so on as an output sequence. Show all design steps. Write verilog program of the same using structural model style. Also write verilog program of all components used in your design.	**14**
		OR	
Q.3		With the help of T-flipflop design a modulo 8 counter. Show all design steps. Write verilog program of the same using structural model style. Also write verilog program of all components used in your design.	**14**
Q.4		Explain the architecture of Spartan3e FPGA family	**14**
		OR	
Q.4		Consider Moore Finite State Machine (FSM), with one input X and one output Z. The FSM asserts its output Z when it recognizes the “10110” input bit sequence. Implement the state diagram for above & write verilog code for it.	**14**
Q.5	**(a)**	Write a verilog program for 16 x 1 multiplexer using conditional operator.	**07**
	(b)	Explain mux- versus LUT-based logic blocks.	**07**
		OR	
Q.5	**(a)**	Write a verilog program for 8 input priority encoder.	**07**
	(b)	Compare the following: (1) Tasks and Functions (2) CPLD and FPGA	**07**

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