Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

M. E. - SEMESTER – II • EXAMINATION – WINTER 2012

Subject code: 1710412 Date: 02/01/2013

Subject Name: Digital VLSI Design

Time: 02.30 pm – 05.00 pm Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Compare energy band diagram for the components that make up the MOS transistor. Draw and explain energy band diagram of the combined MOS system.	**07**
	(b)	Explain Design Hierarchy and Design Quality.	**07**
Q.2	**(a)**	Define τ_{PHL} and τ_{PLH} for CMOS inverter. Derive τ_{PHL} for CMOS inverter.	**07**
		OR	
	(b)	What is LOCOS technique ? Why it is required ? Explain LOCOS with neat sketches.	**07**
	(b)	Write short note on MOSFET scaling.	**07**
Q.3	**(a)**	Describe Accumulation, Depletion and Inversion process for the MOS system under external bias. Also derive the equation for maximum depletion region depth at the onset of surface inversion.	**07**
	(b)	Explain typical fabrication process of MOSFET.	**07**
		OR	
Q.3	**(a)**	Derive the equation of Drain current (I_D) for an N-channel MOSFET operating in a linear region. Draw the necessary sketch.	**07**
	(b)	Write a detail note on Oxide related MOSFET Capacitances.	**07**
Q.4	**(a)**	Draw resistive load nMOS inverter. Discuss its voltage transfer characteristic with important points. Comment on power and area consideration of resistive load nMOS inverter.	**07**
	(b)	What is Euler path approach. Draw the optimized stick-diagram for the following Boolean function (CMOS Logic), $X = \overline{A(D+E)+BC}$. Explain the importance of Euler path approach.	**07**
		OR	
Q.4	**(a)**	Write short note on Dynamic CMOS circuit techniques.	**07**
	(b)	Write a short note on CMOS Transmission Gate. Explain its usefulness.	**07**
Q.5	**(a)**	Explain the charge sharing problem in DOMINO CMOS logic. How it can be over come, suggest simple solution.	**07**
	(b)	Explain D Flipflop with appropriate diagram and waveforms. Draw MOS transitor level schematic.	**07**
		OR	
Q.5	**(a)**	Explain the basic principle of pass transistor, using Logic "1" transfer event. How it is important in dynamic logic circuits.	**07**
	(b)	Explain NAND Gate using CMOS, pass and CPL logic.	**07**

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