GUJARAT TECHNOLOGICAL UNIVERSITY
M. E. - SEMESTER – I • EXAMINATION – WINTER 2012

Subject code: 712602N   **Date: 09-01-2013**
Subject Name: CMOS Circuit Design-I
Time: 02.30 pm – 05.00 pm   **Total Marks: 70**
Instructions:
1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Discuss Dynamic power consumption in CMOS Inverter.	**07**
	(b)	List all Second order effects and discuss any one in detail.	**07**
Q.2	**(a)**	Draw Source Follower stage and derive voltage gain with consideration of body effect.	**07**
	(b)	Discuss Carry Select Adder for 4 bit and 16 bit.	**07**
		OR	
	(b)	Draw One-bit (left-right) programmable shifter and discuss barrel shifter.	**07**
Q.3	**(a)**	Draw basic differential pair and discuss Qualitative analysis.	**07**
	(b)	For W/L =50/0.5, plot the drain current of an NFET and a PFET as a function of $|V_{GS}|$ varies from 0 to 3 volt. Assume $|V_{DS}|$ =V_{DD}=3 volt. Take suitable data from the table given below:	**07**

Table for NMOS Model and PMOS Model

NMOS model			
LEVEL = 1	VTO = 0.7	GAMMA= 0.45	PHI = 0.9
NSUB= 9e+14	LD = 0.08e-6	UO = 350	LAMBDA= 0.1
TOX = 9e-9	PB = 0.9	CJ = 0.56e-3	CJSW=0.35e-11
MJ = 0.45	MJSW = 0.2	CGDO = 0.4e-9	JS = 1.0e-8
PMOS model			
LEVEL = 1	VTO = -0.8	GAMMA = 0.4	PHI = 0.8
NSUB= 5e+14	LD = 0.09e-6	UO = 100	LAMBDA = 0.2
TOX = 9e-9	PB = 0.9	CJ = 0.94e-3	CJSW= 0.32e-11
MJ = 0.5	MJSW = 0.3	CGDO = 0.3e-9	JS = 0.5e-8

OR

Q.3	**(a)**	Discuss Multipole Systems and Phase Margin in brief.	**07**
	(b)	Draw high frequency model of a Cascode stage and discuss the same.	**07**
Q.4	**(a)**	How to suppress the effect of channel-length modulation in Cascode current mirrors. Also discuss Cascode current mirrors.	**07**
	(b)	Discuss Run -Time Power Management, with Dynamic Supply Voltage Scaling (DVS) and Dynamic Threshold Scaling (DTS).	**07**
		OR	
Q.4	**(a)**	Discuss CS stage with source degeneration	**07**
	(b)	Explain the following: (1) Noise Margin (2) Performance parameters of an Op-amp	**07**
Q.5	**(a)**	Discuss Two stage Op-amps.	**07**
	(b)	Discuss Various capacitances in cascaded CMOS Inverter.	**07**
		OR	
Q.5	**(a)**	Draw and discuss different steps, which leads to design of Gilbert cell and explain it.	**07**
	(b)	Discuss Active Current Mirrors.	**07**

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