Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

M. E. - SEMESTER – I • EXAMINATION – WINTER 2012

Subject code: 714103N Date: 12/01/2013

Subject Name: Digital Signal Processor Architecture

Time: 02.30 pm – 05.00 pm Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1 **(a)** Compute DTFT of following signal and sketch its magnitude spectrum. **07**

$$x[n] = \begin{cases} 1, & 0 \le n \le 4 \\ 0, & \text{Otherwise} \end{cases}$$

(b) Define following terms with reference to DSP system: **07**

(1) Iteration period (2) Throughput (3) Latency

Q.2 **(a)** List the major architectural features used in a digital signal processor to achieve high speeds of program execution. **07**

(b) Compare digital signal processors and general purpose microprocessors. **07**

OR

(b) It is required to find the sum of 64 numbers each represented by 16 bits. **07**

(1) How many guard bits should the accumulator have to avoid overflow?

(2) If it is decided to have an accumulator with only 16 bits. But use of shifter is allowed to prevent overflow. By how many bits should each number be shifted?

(3) If all the numbers in part (2) are fixed-point integers, how is the actual sum of numbers related with the contents of the accumulator?

Q.3 **(a)** List and explain any three characteristics of a typical DSP system. **07**

(b) What values are represented by the following 16-bit fixed-point numbers in the Q7 and Q15 notations? **07**

(1) $N = 2000\ H$

(2) $N = 4000\ H$

OR

Q.3 **(a)** Write an algorithm to perform convolution on a digital signal processor with single MAC unit. **07**

(b) Find the product of the following numbers when represented by 4-bits in Q3 format. **07**

(1) 0.5 and 0.25

(2) -0.5 and -0.5

Q.4 **(a)** Explain the pipeline operation for following program of TMS320C5x: **07**

```
        ZAP
        B PGM1250H
        ADD *
        SACL *+
        MAC 4500 H, 25 H
PGM1250H: LACC *+
```

(b) Write TMS320C5X assembly program to add two 64-bit numbers stored in memory. Store the sum in memory. **07**

OR

Q.4 **(a)** Using block diagram, explain central arithmetic logic unit (CALU) of TMS320C5x. **07**

(b) Write TMS320C5X assembly language program to exchange the contents of two data blocks of 10 data values starting from 1000 *H* and 1100 *H*. **07**

Q.5 **(a)** Draw block diagram of CPU unit of TMS320C6x and explain register files in detail. **07**

(b) List and explain the steps involved in 'C6x code generation using CCS tool. **07**

OR

Q.5 **(a)** List and mention the functions of interrupt control registers of TMS320C6713. **07**

(b) Explain the meaning of load/store architecture. List different addressing types for indirect address generation on TMS320C6000. **07**

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