Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

M.E-1st SEMESTER–EXAMINATION –JANUARY-2013

Subject code: 714201N **Date: 08/01/2013**

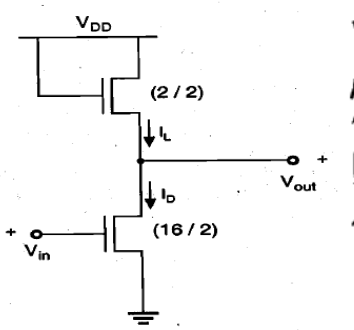
Subject Name: Principles of VLSI Design

Time:02:30 pm – 05:00 pm **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Explain the VLSI Design Flow.	**07**
	(b)	Draw and Explain the Fabrication Steps for NMOS.	**07**
Q.2	**(a)**	Explain The Voltage Transfer Characteristic of Resistive Load NMOS Inverter.	**07**
	(B)	Explain The Significance of Photolithography and Multilevel Metallization in Fabrication.	**07**
		OR	
	(B)	What is Layout Design Rules? Explain in Detail.	**07**
Q.3	**(a)**	For the Inverter Given in figure1 Calculate V_{OH}, VOL, VIL and NM_L.	**07**



$V_{T0} = 0.8$ V
$\mu_n C_{ox} = 45.0\ \mu A/V^2$
$\gamma = 0.38\ V^{1/2}$
$|2\ \phi_F| = 0.6$ V
$\lambda = 0$
$V_{DD} = 5.0$ V

(Figure 1)

	(b)	Draw the Stick Diagrams For Following Logic Function. I. F= A'B + AB'. II. F= (AB)'. III. F= (A+B)'.	**07**
		OR	
Q.3	**(a)**	Explain the Delay Time T_{PHL} and T_{PLH} for CMOS Inverter.	**07**
	(b)	What is Scaling? Explain the Small Geometry Effects.	**07**
Q.4	**(a)**	Draw and explain the CMOS Inverter with all paratactic capacitance and derive the equation of C_{Load}.	**07**
	(b)	Describe the Two Input NOR Gate with CMOS Inverter with Necessary Equations.	**07**
		OR	
Q.4	**(a)**	Implement the Following Boolean Function by Using Transmission Gate. I. F= AS'+BS. II. F=AB'+A'B. III. F=AB+A'C'+AB'C.	**07**
Q.4	**(b)**	Describe the BiCMOS Inverter.	**07**

Q.5	**(a)**	Draw and Explain the Depletion-Load NMOS SR Latch Circuit Based on NOR2 Gate.	**07**
	(b)	Implement the D-Latch by Using CMOS and Explain in Detail	**07**
		OR	
Q.5	**(a)**	Describe the Dynamic CMOS Logic.	**07**
	(b)	Draw and Explain the AOI Based Clocked NOR Gate Based SR Latch Circuit.	**07**

****