

GUJARAT TECHNOLOGICAL UNIVERSITY**M. E. - SEMESTER – I • EXAMINATION – WINTER 2012****Subject code: 714205N****Date: 10-01-2013****Subject Name: Advanced Digital Design (Minor Elective – I)****Time: 02.30 pm – 05.00 pm****Total Marks: 70****Instructions:**

1. Attempt all questions.
2. Make suitable assumptions wherever necessary.
3. Figures to the right indicate full marks.

- Q.1** (a) Explain Full Subtractor using two half subtractor. **07**
(b) Create AND, OR, NOT gate using NOR gate and explain it in detail. **07**
- Q.2** (a) Simplify the following Boolean function by using k map and draw its gate level diagram. **07**
 $F = \Sigma (0, 1, 2, 8, 10, 11, 14, 15)$
(b) Draw SR and JK flip flop with its truth table. **07**
- OR**
- (b) Explain importance of memory, register and counter in detail with its important. **07**
- Q.3** (a) Draw AND gate using CMOS with truth table and explain it in detail. **07**
(b) Explain stuck at fault in testability with suitable example. **07**
- OR**
- Q.3** (a) Draw EX-OR gate using NAND gate and explain it for fault finding. **07**
(b) Explain fault diagnosis and explain steps to minimize it. **07**
- Q.4** (a) Explain PLA logic with suitable example. **07**
(b) Write VHDL code for 4 x 1 Multiplexer. **07**
- OR**
- Q.4** (a) Give brief detail of VHDL coding and its types. **07**
(b) Write VHDL code for 3 to 8 Decoder. **07**
- Q.5** (a) Draw INVERTER using CMOS and write SPICE codes for it. **07**
(b) What are CPLD and FPGA give its detail. **07**
- OR**
- Q.5** (a) Give detail of low power design with its performance. **07**
(b) Draw CMOS NAND and NOR Gate with respective truth table. **07**
