Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

M. E. - SEMESTER – I • EXAMINATION – WINTER 2012

Subject code: 715202 **Date: 09-01-2013**

Subject Name: Digital VLSI Design – I Frontend

Time: 02.30 pm – 05.00 pm **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Compare and contrast directed test and random test in Verilog with suitable examples	**07**
	(b)	Explain differences between blocking & non-blocking assignments, continuous & procedural assignments in Verilog with suitable examples	**07**
Q.2	**(a)**	What is meant by verification? Explain the importance of constraint driven verification. How is it different from directed testing? Illustrate with suitable examples	**07**
	(b)	What is meant by interface? What are the different types of interfaces? Explain the significance of mod ports, clocking blocks and signal declarations in interface with suitable examples	**07**
		OR	
	(b)	Explain the following: task and function, $display and $monitor, rand and randc, symbol library and target library	**07**
Q.3	**(a)**	Explain the top down and bottom up design approaches in VSLI design with suitable examples	**07**
	(b)	Design a 4:1 multiplexer using 2:1 multiplexer. Draw the block diagram, truth table and timing diagram for the same	**07**
		OR	
Q.3	**(a)**	Explain the following terms in ASIC design flow : Design specification, Functional Verification, Synthesis , Logical verification and Fabrication	**07**
	(b)	What is Moore's law? Explain its significance with respect to following : transistor count, die size growth, frequency, power dissipation	**07**
Q.4	**(a)**	What is meant by coverage? Explain the importance of coverage in random testing. Briefly explain line coverage, branch coverage, toggle coverage, FSM coverage and conditional coverage	**07**
	(b)	Write a Verilog RTL for a 2 to 4 decoder. Develop directed and random test benches for the same	**07**
		OR	
Q.4	**(a)**	Design 4 bit ripple carry adder. Draw the block diagram, truth table, timing diagram and write the Verilog RTL for the design	**07**
Q.4	**(b)**	Write interface, random test bench with constraints and coverage plan in system Verilog for the above design	**07**
Q.5	**(a)**	What is a finite state machine? Explain the differences between Mealy and Moore state machine. Design a Moore FSM for the sequence 10001. Draw the state transition table, state transition diagram and signal descriptions	**07**

	(b)	For the above FSM, write the Verilog RTL and complete system Verilog test bench	**07**

OR

Q.5	**(a)**	What are the differences between synchronous and asynchronous state machines? Design a simple mealy FSM for the sequence 11010. Write the Verilog RTL for the FSM	**07**
	(b)	List Verilog coding guide lines for efficient design with reasons and examples. Illustrate the differences between one hot encoding and binary encoding in state machine design	**07**

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