Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

M. E. - SEMESTER – II • EXAMINATION – WINTER • 2013

Subject code: 1710412 Date: 02-01-2014

Subject Name: Digital VLSI Design

Time: 10.30 am – 01.00 pm Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1 **(a)** Answer the following questions in short. (Two mark each) **14**

1. For 90nm process what is feature size and λ?

2. What is need of SiO2 layer in MOS fabrication process? During CMOS fabrication why etching is used?

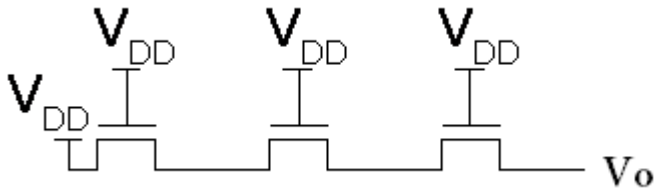
3. Explain Cross talk in Interconnect.

4. Draw 2x1 MUX using transmission gate.

5. Compare SRAM and DRAM cell for size, power dissipation and speed.

6. Consider 5mm long, 0.32µm wide metal2 wire in 180nm process. The sheet resistance is 0.05Ω/□ and the capacitance is 0.2fF/µm. Calculate wire resistance and capacitance.

7. For the NMOS pass transistor circuit shown in figure 1 below, find Vo.



(Figure 1)

Q.2 **(a)** Explain types of photoresists and their usage in lithography process with appropriate diagram. **07**

(b) Discuss Static and Dynamic power dissipation of CMOS inverter. **07**

OR

(b) Explain Complementary pass transistor logic (CPL). With diagram explain 2 input NOR and XOR gate using CPL. **07**

Q.3 **(a)** Explain current equations for three regions of operation of NMOS transistor with internal diagram of NMOS transistor. Also draw I-V characteristic of NMOS transistor. **07**

(b) Discuss Short channel effect in MOSFET with diagram. **07**

OR

Q.3 **(a)** Show internal diagram of MOS transistor and explain calculation of gate capacitance. With diagram show variation of the gate capacitances as functions of gate-to- **07**

source voltage V_{GS}

(b) Explain the nMOS and pMOS enhancement transistor with its physical structure **07**

Q.4 **(a)** Consider a CMOS I nverter with V_{DD} = 3.3 V. The I-V characteristics of the NMOS transistor are specified as: when V_{GS} = 3.3V, the drain current reaches its satuaration level Isat = 2mA for VDS $\geq$ 2.5V. Input signal applied to gate is ideal step pulse. Calculate delay time necessary for the output to fall from its initial value of 3.3V to 1.65V assuming output load capacitance of 300f. Derive equations which you have used. **07**

(b) Draw and explain voltage transfer characteristic of CMOS inverter and discuss noise margin. **07**

OR

Q.4 **(a)** CMOS fabrication device parameters are listed below. **07**

$\mu_n C_{ox}$= 120μA/V^2

$\mu_p C_{ox}$= 60 μA/V^2

$V_{TO,n}$=0.8V

$V_{TO,p}$= -1.0V

V_{DD} = 3.3V

L =0.6μm for both NMOS and PMOS devices.

Design a CMOS inverter by determining the channel widths W_n and W_p of the NMOS and PMOS trasistor to meet the specifications of propagation delay times $\tau_{PHL} \leq 0.2$ns and $\tau_{PLH} \leq 0.15$ns.

Assume load capacitance of 300fF and ideal step input.

Q.4 **(b)** Sketch 2 input NAND gate with transistor widths chosen to achieve effective rise and fall resistance equal to a unit inverter. Compute the rising and falling propagation delays in terms of R and C of the NAND gate driving h identical NAND gates using the Elmore delay model. If C = 2fF/μm and R = 2.5KΩ · μm in 180nm process, what is the delay of fanout-of-4 NAND gate? **07**

Q.5 **(a)** Sketch following boolean function using CMOS compound gate with transistor widths chosen to achieve equal effective rise and fall resistance i.e. $(W/L)_{n,eq} = (W/L)_{p,eq}$ **07**

1. $Y_1 = \overline{A\,(B + C) + DE}$
2. $Y_2 = \overline{ABC}$

(b) Discuss cascading problem in dynamic CMOS logic circuit with appropriate diagram. **07**

OR

Q.5 **(a)** Draw Stick diagram of 3-input NAND gate and 3-input NOR gate. **07**

(b) With diagram explain 1 bit full adder using transmission gates. **07**

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