Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

M. E. - SEMESTER – I • EXAMINATION – WINTER • 2013

Subject code: 710403N Date: 03-01-2014

Subject Name: ASIC Design

Time: 10.30 am – 01.00 pm Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1 **(a)** List All eight types of ASICs and discuss any two of them in detail. **07**

(b) For Floor planning process whether following statements are true or false? Justify your answer. **07**

1) Floor planning can be used for arranging the blocks on a chip.
2) Floor planning can describe interconnection within the blocks.
3) Floor planning is mapping between physical description to logical description.
4) Decide location and number of power pads.
5) Decide type of power distribution.
6) Decide location but not decide type of clock distribution.
7) The objectives of floor planning are to minimize chip area but not delay.

Q.2 **(a)** Give details related to Xilinx XC3000 programmable ASIC. **07**

1) Basic logic cell.
2) Logic cell contents
3) Logic path delay
4) Combinational Logic functions
5) Flip flop implementation
6) Basic logic cell in each chip

(b) What is an OTP FPGAs? How it differs from other FPGAs? Compare FPGA and CPLD. **07**

OR

(b) 1) What are the objectives of placement? **03**

2) What is postponed processes? Explain giving example. **04**

Q.3 **(a)** Define following terms: 1) Uncommitted feed through **07**
2) feed through 3) Postponed process 4) Routing
5) Inertial delay 6) Basic Identifiers 7) Delta Delay

(b) 1) Give difference between signal and variable. **04**

2) Differentiate between concurrent and sequential signal assignment statement. **03**

OR

Q.3 **(a)** What is signal driver? When multiple drivers exist for any signal? What is the solution for assignment of new value to any signal in case of multiple drivers? **07**

(b) Explain with a diagram the architecture of CLB's available in Xilinx FPGA. **07**

Q.4 **(a)** What is the use of attribute in VHDL? Describe all the attributes in detail. **07**

	(b)	Write a code for ALU in VHDL for eight different operations.	**07**

OR

Q.4	**(a)**	Discuss Moore and Mealy state Machine with example.	**07**
	(b)	Using structural modeling write a VHDL code for Bidirectional universal shift register with parallel load.	**07**
Q.5	**(a)**	Write a VHDL code for Johnson Counter using FSM.	**07**
	(b)	Draw a state diagram for moore type finite state machine which generates output '1' when receives input string sequence '10010' on five subsequent clock cycles. Include Reset signal which bring FSM to initial state when it goes to high. Write VHDL code for this FSM using process statement.	**07**

OR

Q.5	**(a)**	Write a code in VHDL using behavioral method for 4X4 switch with 10 bit input in which 8 bits are data bits and 2 bits for selecting output line. All four outputs are of 8 bits. Priority need to assign to all the inputs.	**07**
	(b)	Using structural method write a VHDL code for (4-bit) binary parallel adder. Take 1-bit Full adder as a component.	**07**

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