Seat No.: _____ *Enrolment No._____*

GUJARAT TECHNOLOGICAL UNIVERSITY

M. E. - SEMESTER – I • EXAMINATION – WINTER • 2013

Subject code: 710412N **Date: 08-01-2014**

Subject Name: Digital VLSI Design

Time: 10.30 am – 01.00 pm **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Draw the VLSI design flow in terms of Y-chart. Discuss the each three domain of Y-chart in detail.	**07**
	(b)	Explain CMOS fabrication process with necessary diagram	**07**
Q.2	**(a)**	Explain two types of scaling with its advantages and disadvantages.	**07**
	(b)	Explain the need for LOCOS Process, principle of LOCOS and LOCOS process with necessary diagram.	**07**
		OR	
	(b)	Explain types of photoresists and their usage in lithography process with appropriate diagram.	**07**
Q.3	**(a)**	Derive the equation of Drain current (I_D) for an N-channel MOSFET operating in a linear region. Draw the necessary sketch.	**07**
	(b)	Draw and explain voltage transfer characteristic of CMOS inverter and discuss noise immunity and noise margin.	**07**
		OR	
Q.3	**(a)**	Consider a resistive-load inverter circuit with V_{DD}= 5V, kn'= 22μA/V^2, V_{T0}= 0.8 V, R_L= 200 k, and W/L = 2. Calculate the critical voltages (V_{OL},V_{OH}, V_{IL},V_{IH}) on the VTC and find the noise margins of the circuit.	**07**
	(b)	Derive expressions for τ_{PHL} and τ_{PLH} using differential equation method.	**07**
Q.4	**(a)**	What is clock skew problem for NP-Domino CMOS Logic circuits? Explain. True Single Phase Clock (TSPC) Dynamic CMOS Logic circuits.	**07**
	(b)	Derive the switching threshold (V_{th}) for CMOS inverter. Also prove that for symmetric inverter $\left(\frac{W}{L}\right)_p \approx 2.5\left(\frac{W}{L}\right)_n$	**07**
		OR	
Q.4	**(a)**	Explain CMOS transmission gate and design 4X1 Mux using transmission gate.	**07**
	(b)	Explain the Euler path approach to find the optimized stick-diagram for any CMOS logic circuit. Take suitable example to justify your answer.	**07**
Q.5	**(a)**	Explain the basic principle of pass transistor, using Logic "1" transfer event. How it is important in dynamic logic circuits.	**07**
	(b)	Draw and explain CMOS SR latch circuit based on NOR2 gates.	**07**
		OR	
Q.5	**(a)**	Explain basic principles of pass transistor circuits.	**07**
	(b)	Short note on FPGA.	**07**

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