Seat No.:	Enrolment No.

GUJARAT TECHNOLOGICAL UNIVERSITY M. E. - SEMESTER – I • EXAMINATION – WINTER • 2013

Sul Tir	bject ne: 1 struc 1. 2.	Code: 712601N Name: Digital Signal Processing Algorithm & Processor Architecture 0.30 am – 01.00 pm Total Marks: 70 etions: Attempt all questions. Make suitable assumptions wherever necessary. Figures to the right indicate full marks.	
Q.1	(a)		07
	(b)	(iii) Time Variant – Time Invariant discrete time systems. Perform circular and linear convolution of the sequences $x(n)=\{2,1,2\}$ and $y(n)=\{2,3\}$ using graphical method. Make suitable comment about result.	07
Q.2	(a)	Find the impulse response, frequency response and magnitude response of $\frac{3}{2}$	07
	(b)	$y(n) - y(n-1) + \frac{3}{16}y(n-2) = x(n) - \frac{1}{2}x(n-1)$ Determine the causal signal x(n) having the z-transform	07
	(6)	$\frac{1}{(1+z^{-1})(1-z^{-1})^2}$	07
		OR	
	(b)	Realize the following in parallel form. $H(z) = \frac{(1+z^{-1})(1+2z^{-1})}{\left(1+\frac{1}{8}z^{-1}\right)\left(1-\frac{1}{2}z^{-1}\right)^2\left(1-\frac{1}{4}z^{-1}\right)}$	07
Q.3	(a)	Design a linear phase FIR high pass filter using hamming window with cutoff frequency 0.8π rad/sample and N=7. Given Frequency response $H_{\rm d}(\omega)=e^{-j\omega\alpha}$, $\omega_c\leq \omega \leq \pi$	07
	(b)	= 0 , otherwise Explain the Energy Density Spectrum, Power Spectrum and Periodogram. OR	07
Q.3	(a)	Design Digital butterworth filter that satisfy the following constraint using bilinear transformation. Assume Ts= 1s. $0.9 \le H(\omega) \le 1$, $0 \le \omega \le \frac{\pi}{2}$ and $ H(\omega) \le 0.2$, $\frac{3\pi}{4} \le \omega \le \pi$	07
	(b)	Explain the fundamentals of Discrete Wavelet Transform.	07
Q.4	(a) (b)	Explain the Time reversal and Circular time shift properties of DFT. Find out 8-point FFT of sequence $x(n) = \{1,2,1,2\}$ using DIF.	07 07
Q.4	(a) (b)	Explain overlap save method of linear filtering. Determine the IDFT of sequence $X(k)=\{3,2+j,1,2-j\}$.	07 07
Q.5	(a) (b)	Explain the features of Digital Signal Processor in brief. Explain the C5X processor pipeline operation on ARAU memory mapped registers.	07 07
Q.5	(a) (b)	OR Explain the execution unit of TMS320C5X processor. Explain the features and internal architecture of TMS320C6X processor. ***********************************	07 07