Seat No.: _____ *Enrolment No._____*

GUJARAT TECHNOLOGICAL UNIVERSITY

M. E. - SEMESTER – I • EXAMINATION – WINTER • 2013

Subject code: 714103N **Date: 03-01-2014**

Subject Name: Digital Signal Processor Architecture

Time: 10.30 am – 01.00 pm **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Explain following terms with reference to DSP system: (1) Iteration period (2) Throughput (3) Latency	**07**
	(b)	Compare digital signal processors and general purpose microprocessors.	**07**
Q.2	**(a)**	Enlist advantages of DSP systems over analog systems. Also explain the role of analog circuits in DSP systems.	**07**
	(b)	Using FIR filter equation, explain the demands of DSP algorithms. How programmable digital signal processors meet these demands?	**07**
		OR	
	(b)	Compute DTFT of following signal and sketch its magnitude spectrum. $x[n] = 1, 0 \leq n \leq 4$, otherwise it is 0.	**07**
Q.3	**(a)**	In a CD player, the sampling rate is 44.1 kHz, and each audio sample is quantized to 16 bits. If the CD player requires a 300-tap FIR filter, what kind of DSP processors has an adequate million instructions-per-second (MIPS) rating to perform this task? What is the size of memory required to store up to 30 minutes of digitized stereo signal?	**07**
	(b)	Compare RISC and CISC processors.	**07**
		OR	
Q.3	**(a)**	A non-pipeline system takes 100 ns to process a task. The same task can be processed in a 5-stage pipeline with the time delay of each segment in the pipeline is given as 20ns, 25ns, 30ns, 10ns, and 15ns. Determine the speed-up ratio of the pipeline for 10, 100, and 1000 tasks. What is the maximum speed-up that can be achieved?	**07**
	(b)	List and explain finite-word length effects.	**07**
Q.4	**(a)**	Write an algorithm to perform convolution on a digital signal processor with single MAC unit.	**07**
	(b)	Write TMS320C5X assembly program to add two 64-bit numbers stored in memory. Store the sum in memory.	**07**
		OR	
Q.4	**(a)**	Explain various on-chip peripherals in TMS320C5X.	**07**
	(b)	List bits of status register 0 (ST0) of TMS3205X and their functions.	**07**
Q.5	**(a)**	Explain the meaning of load/store architecture. List different addressing types for indirect address generation on TMS320C6000.	**07**
	(b)	Write TMS320C5X assembly language program to exchange the contents of two data blocks of 10 data values starting from 1000 *H* and 1100 *H*.	**07**
		OR	
Q.5	**(a)**	List and explain the steps involved in ‘C6x code generation using CCS tool.	**07**
	(b)	List and mention the functions of interrupt control registers of TMS320C6713.	**07**

****