Seat No.: _____ *Enrolment No._____*

GUJARAT TECHNOLOGICAL UNIVERSITY

M. E. - SEMESTER – I • EXAMINATION – WINTER • 2013

Subject code: 714201N **Date: 23-12-2013**

Subject Name: Principles of VLSI Design

Time: 10.30 am – 01.00 pm **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full mark.**

Q.1 **(a)** Explain in detail : VLSI Design Flow **07**

(b) Compare Followings : **07**

(i) Full Custom Design and Semi Custom Design

(ii) ASIC and FPGA

Q.2 **(a)** Explain the basic steps of fabrication with necessary figures. **07**

(b) Draw & explain VTC of CMOS Inverter. Derive the necessary equation for the same. **07**

OR

(b) Design a resistive-load inverter with R = 1 kΩ, such that V_{OL} = 0.6 V. The enhancement-type nMOS driver transistor has the following parameters: **07**

V_{DD} = 5 V, V_{TO}= 1V, $\gamma = 0.2\ V^{1/2}$, λ=0.0 V^{-1}, $\mu_n C_{ox} = 22.0\ \mu A/V^2$

(a) Determine the required aspect ratio, W/L.

(b) Determine V_{IL} and V_{IH}.

(c) Determine noise margins N_{ML} and N_{MH}.

Q.3 **(a)** What is Photoresist? Why it is used in fabrication of IC? How many types of Photoresist? Explain each in detail and also give the comparison between them. **07**

(b) Explain noise margin & noise immunity in case of three inverter in cascade form. **07**

OR

Q.3 **(a)** Write a short note CMOS ring oscillator. **07**

(b) Derive expression for T_{PHL} & T_{PLH} for CMOS inverter. **07**

Q.4 **(a)** Explain CMOS Transmission Gate. **07**

(b) Explain in detail NORA CMOS Logic. **07**

OR

Q.4 **(a)** Explain Logic '1' transfer for Pass Transistor Circuit **07**

(b) Explain with necessary derivation Voltage Bootstrapping. **07**

Q.5 **(a)** Explain in brief BiCMOS. **07**

(b) Explain in detail True Single Phase Clock Dynamic CMOS **07**

OR

Q.5 **(a)** Explain CMOS SR Latch based on NOR Gate. **07**

(b) Explain CMOS AOI realization of JK Latch. **07**

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