Seat No.: _____ *Enrolment No._____*

GUJARAT TECHNOLOGICAL UNIVERSITY

M. E. - SEMESTER – I • EXAMINATION – WINTER • 2013

Subject code: 714205N **Date: 30-12-2013**

Subject Name: Advance Digital Design

Time: 10.30 am – 01.00 pm **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full mark.**

Q.1	**(a)**	Explain NAND and NOR as a universal gate with examples.	**07**
	(b)	Design BCD to Excess-3 code converter with gates.	**07**
Q.2	**(a)**	Implement Boolean expression for Ex-OR gate using NAND gates only.	**07**
	(b)	Draw the truth table and Logic diagram of full subs tractor.	**07**
		OR	
	(b)	Simplify the Boolean function: $F(w,x,y,z) = \Sigma (2,3,4,10,11,12)$	**07**
Q.3	**(a)**	What is Asynchronous design explain in detail.	**07**
	(b)	Draw logic diagram, graphical symbol, and Characteristic table for clocked D flip- flop.	**07**
		OR	
Q.3	**(a)**	With logic diagram and truth table explain the working JK Flip-flop. Also obtain its Characteristic equation.	**07**
	(b)	Write VHDL code for 3 to 8 Decoder.	**07**
Q.4	**(a)**	Write VHDL code for Half Adder & Full Adder.	**07**
	(b)	Explain Testability with one example.	**07**
		OR	
Q.4	**(a)**	Explain Design Procedure for Combinational Circuit & Difference between Combinational Circuit & Sequential Circuit	**07**
	(b)	Explain counter in detail with one example.	**07**
Q.5	**(a)**	Explain PLD in detail with its advantages.	**07**
	(b)	Write SPICE code for CMOS NAND gate.	**07**
		OR	
Q.5	**(a)**	Explain FGPA in detail with examples.	**07**
	(b)	Write SPICE code for CMOS NOR gate.	**07**

****