GUJARAT TECHNOLOGICAL UNIVERSITY
M. E. - SEMESTER – I • EXAMINATION – WINTER • 2013

Subject code: 715404   **Date: 01-01-2014**
Subject Name: Advanced Digital Circuit Design
Time: 10.30 am – 01.00 pm   **Total Marks: 70**
Instructions:
1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Discuss difference between modules and module instances.	**07**
	(b)	Discuss data types used in verilog in brief.	**07**
Q.2	**(a)**	List various operator types. Discuss any one in detail.	**07**
	(b)	Draw the block-diagram and write verilog code for 4 bit ripple carry full adder using 4 one bit full adders.	**07**

OR

	(b)	Draw the block-diagram and write verilog code for ripple counter using 4 T flip-flop.	**07**
Q.3	**(a)**	Discuss delay based timing control in verilog.	**07**
	(b)	Discuss differences between tasks and functions.	**07**

OR

Q.3	**(a)**	Discuss event based timing control in verilog.	**07**
	(b)	Discuss overriding parameters in modeling techniques in verilog.	**07**
Q.4	**(a)**	Discuss partitioning in brief.	**07**
	(b)	How to detect static hazard in Multi Level Network?	**07**

OR

Q.4	**(a)**	Discuss placement and routing in brief.	**07**
	(b)	What is hardware software co-design? Explain in brief.	**07**
Q.5	**(a)**	Explain steps for Finite state machine design procedure.	**07**
	(b)	How many different encodings are possible for a four-state finite state machine? List and discuss different encoding strategies for state assignments.	**07**

OR

Q.5	**(a)**	Discuss concept of floor planning in brief.	**07**
	(b)	Explain Built in self test.	**07**

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